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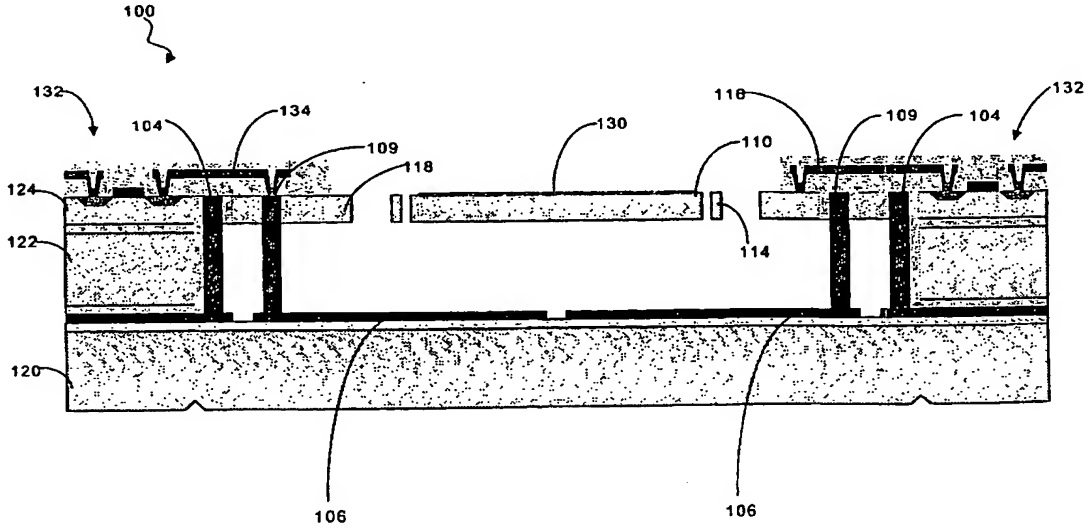
(54) Title: BONDED WAFER OPTICAL MEMS PROCESS




(57) Abstract: A microelectromechanical system is fabricated from a substrate having a handle layer, a silicon sacrificial layer and a device layer. A micromechanical structure is etched in the device layer and the underlying silicon sacrificial layer is etched away to release the micromechanical structure for movement. One particular micromechanical structure described is a micromirror.

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# BONDED WAFER OPTICAL MEMS PROCESS

## PRIORITY INFORMATION

## BACKGROUND OF THE INVENTION

The invention relates to the field of microfabricated devices, and in particular to microfabricated devices released to move by removal of a sacrificial layer.

Microelectromechanical systems (MEMS) have a broad range of applications such as, accelerometers, gyroscopes, visual displays and micro-optical systems for fiber-optic communications. The techniques used to form the micromechanical structures, such as surface micromachining, borrow technologies like thin film deposition and photolithography from the microelectronics fabrication industry.

In surface micromachining, thin films of material are typically deposited on a surface (typically known as the handle layer) using a variety of methods to form a device layer of material on a sacrificial layer of material. The micromechanical structure is then formed by patterning and etching the device layer. After the micromechanical structure is formed, a release etch is performed to remove the sacrificial material so that the micromechanical structure is released, allowing it to move and perform mechanical functions.

One actuation scheme used to move the micromechanical structure or otherwise cause it to perform its mechanical function is electrostatic actuation. Electrostatic actuation is commonly used because it does not require complicated fabrication techniques or abnormal materials, such as piezoelectric materials. Electrostatic actuation moves the micromechanical structure by electrostatic attraction between two structures with different voltages applied thereto. When the voltages are applied, the structures move to increase their capacitance by increasing the overlap area of overlapping features, or by closing the gap between the overlapping features.

Because surface micromachining lends itself naturally to creating overlapping surfaces coupled, at least in part, with the common use of electrostatic actuation has resulted in the development of a micromechanical structure used in a number of diverse applications, such as micromirrors, accelerometers, gyroscopes, etc. This structure comprises a plate formed in the device layer that is coupled via flexure assemblies to a frame formed in the device layer. The plate is released to suspend above the handle layer by the removal of the sacrificial layer underlying the plate.

The distance between the plate and the handle layer, however, limits the actuation range of the plate in this structure. This distance directly corresponds to the thickness of the sacrificial layer. An oxide, such as silicon dioxide is typically used as the sacrificial layer. An oxide, however, cannot be grown sufficiently thick to provide the desired actuation range for some applications of this structure.

One such application is micro-optical structures, such as micromirrors. While small deflections suffice for some micromirrors, large micromirrors (greater than about 300 um in diameter) require mirror rotations in the tens of microns (e.g., between about 50-80um) to be useful. An oxide generally cannot provide for the needed separation between the device layer and the handle layer for such mirror rotations. Therefore, most large micromirrors are not made using the above-described structure. Alternative structures for large micromirrors, such as assembled, hinged or bimorph pop-up structures, have a number of disadvantages. They are often difficult to fabricate, are unreliable, provide low-yield and are many times unmanufacturable devices.

Prior art processes for forming micromirrors also suffer from other disadvantages. For example, many require a through-wafer etch to access the backside of structure. These through- wafer etches create fragile final chips. Etch holes through the mirror surface are often required for the release etch. These etch holes increase signal loss due to scattering. In addition, the prior art processes are not easily integrated with foundry electronics and cannot provide a single chip solution, i.e. one where no assembly is required of separate mirror and electronics chips. The prior art forms micro-optic MEMS systems by constructing the mirror structure on one chip, the electronics on a second chip and then using wire bonding to interface the two components to form the micro-optic system. Integration of active electronics on the same wafer as a micro-optical structure would provide a number of advantages.

## SUMMARY OF THE INVENTION

In one aspect of the present invention, a method of fabricating a microelectromechanical system is provided. First, a substrate is provided that comprised a handle layer of silicon, a device layer of silicon and a sacrificial layer of silicon disposed between the handle layer and the device layer. Next, a micromechanical structure is formed in the device layer. Then, at least a portion of the sacrificial layer of silicon underlying the micromechanical structure is removed to release the micromechanical structure for movement.

In another aspect of the present invention, a method of releasing a micromechanical structure for movement is provided. The micromechanical structure is etched in a silicon device layer and a silicon sacrificial layer disposed between said micromechanical structure and a silicon handle layer is etched.

Another aspect of the present invention provides a microfabricated device. The microfabricated device comprises a substrate having a device layer; a least one micro-optical device etched on the device layer and released for movement by removal of an underlying sacrificial layer of silicon; and active electronics formed on the device layer.

Provided in another aspect of the present invention is a microelectromechanical device. The device comprises a handle layer of silicon having actuation electrodes formed thereon, a device layer of silicon having a micromechanical structure formed thereon and a sacrificial layer of silicon disposed between the handle layer and the device layer of silicon. The sacrificial layer of silicon has a portion underlying the micromechanical structure removed to form an actuation cavity below the micromechanical structure.

In another aspect, a micromirror device is provided. The micromirror device comprises a substrate having a device layer, a handle layer and a sacrificial layer made of silicon disposed between the device layer and the handle layer and an isolation trench extending through the device layer and the sacrificial layer. The isolation trench defines a mirror region and electrically isolates the mirror region. The micromirror device also comprises a mirror formed from the device layer in the mirror region above actuation electrodes formed on said handle layer. In addition, a cavity is formed below the mirror by removing a portion of said sacrificial layer of silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a-1c illustrate a preferred micromirror structure constructed according to the principles of the present invention in which single crystal silicon is used as the device layer;

Figures 2a-2j illustrate the fabrication steps of the micromirror structure of figures 1a-1c;

Figures 3 illustrates another embodiment of a micromirror structure constructed according to the principles of the present invention in which polycrystalline silicon is used as the device layer; and

Figures 4a-4l illustrate the fabrication steps of the micromirror structure of figure 3.

## DETAILED DESCRIPTION OF THE INVENTION

While the various embodiments of the present invention are described with respect to, and some embodiments are particularly advantageous for, the production of micromirrors, the present invention is not limited thereto. As will be appreciated by one of skill in the art, the principles of the present invention are applicable to a number of other devices, such as inertial sensors, pressure sensors, and actuators.

Figures 1a, 1b and 1c illustrate a preferred micromirror structure **100** constructed according to the principles of the present invention. Figures 1a and 1b illustrate top planar views of different layers of preferred micromirror structure **100**. Figure 1a illustrates a top planar view of the device layer of micromirror structure **100**. Figure 1b illustrates a top planar view of the handle layer of micromirror structure **100**. Figure 1c illustrates a side view of micromirror structure **100**.

Micromirror structure **100** is created from a substrate having a handle layer **120**, a sacrificial layer **122** and a device layer **124**, each separated by a dielectric, such as silicon dioxide. Single crystal silicon is used as sacrificial layer **122** in order to provide for greater distances between mirror **110** and handle layer **120**, and, in turn, a greater actuation range. Handle layer **120** and device layer **124** are also single crystal silicon. Significant advantages are obtained with device layer **124** being single crystal silicon. The use of single crystal silicon as device layer **124** provides for larger, flatter mirrors and provides a substrate that is compatible with traditional CMOS fabrication techniques. This allows for control and processing electronics **132** to be formed directly on the substrate. Therefore, it is possible to integrate active electronics on the same wafer as a micro-optical structure.

As illustrated, a mirror **110**, formed from device layer **124**, is suspended over a cavity created by the removal of sacrificial layer **122** underlying mirror **110**. Mirror **110** has a coating **130** thereon to increase the reflectivity. Mirror **110** is suspended by flexure connections **112**. Preferably, mirror **110** is connected to a concentric suspension ring **114** via a first set of flexures **112a** and concentric suspension ring **114** is connected to frame **118** via a second set of orthogonally oriented flexures **112b**. Preferably, flexures **112** are serpentine structures as illustrated in figure 1d, which shows a close-up of one of the set of flexures **112b**.

An isolation trench **104** extends down to handle layer **120** from device layer **124** and surrounds the area containing mirror **110** and associated frame **118**. Isolation trench **104** electrically isolates micromirror structure **100** from the rest of the wafer. Further, as will be seen below, isolation trench **104** also acts as a lateral etch stop for

the sacrificial layer etch and provides a mechanical anchor for mirror **110**.

Similar to isolation trench **104**, via posts **109**, filled with a conductive material such as doped polysilicon, extend through contact holes **108** down to handle layer **120** from device layer **124**. Via posts **109** connect to interconnects **106** formed on handle layer **120**. Interconnects **106** have pads at one end for connection to via posts **109** and are connected at the other end to actuation electrodes **121** formed on handle layer **120**. An electrical interconnection **116** formed on top of the device layer is used to apply a first voltage to the device layer of micromirror structure **100**. Electrical interconnections **134** connected to via posts **109** are then used to apply a second voltage to actuation electrodes **121** to move mirror **110**.

Referring to figures 2a and 2b, the fabrication process for micromirror structure **100** begins with a single crystal silicon wafer **222** bonded using wafer bonding to a single crystal silicon wafer **220**, which has interconnects and actuation electrodes **206** formed thereon. Interconnects and actuation electrodes **206** are preferably formed using patterned polysilicon. However, other manners of forming interconnects and actuation electrodes **206**, such as patterned diffusions into wafer **220**, are possible. Alternatively, interconnects and electrodes **206** may be formed on the bottom of wafer **222**. Wafer **222** is ground to the desired sacrificial layer thickness (e.g., 50 um) using, for example, a combination of mechanical and chemical-mechanical polishing (CMP). A second wafer **224** is then bonded, also using wafer bonding, to wafer **222** and ground to the desired thickness (e.g., 10 um) of the mechanical structure and the circuits, also using, for example, a combination of mechanical and chemical-mechanical polishing (CMP).

This results in a substrate **200** comprised of a handle layer **220** of single crystal silicon, a sacrificial layer **222** of single crystal silicon and a device layer **224** of single crystal silicon. A first dielectric layer **203** separates sacrificial layer **222** and handle layer **220** and a second dielectric layer **205** separates device layer **224** from sacrificial layer **222**.

While described as being formed from three bonded silicon wafers, alternative techniques of forming three-layer substrate **200** are possible. One possible alternative entails wafer bonding a single silicon-on-insulator (SOI) wafer to dielectric layer **203** on wafer **220**. In this case, the silicon layer of the SOI wafer above the insulator is made to be the appropriate thickness before bonding and is sacrificial layer **222**. The handle layer of the SOI wafer is device layer **224** and is ground to the appropriate

thickness after bonding.

Another possible alternative entails double bonding of two SOI wafers to wafer **220**. For this technique, a SOI wafer is bonded to wafer **220** and the handle layer of the SOI wafer is removed. This leaves sacrificial layer **222** and dielectric **205**. A second SOI wafer is then wafer bonded on top of dielectric **205**. The handle layer and insulator layer of the second SOI wafer is then removed to leave device layer **224**.

Referring next to figures 2b and 2c, after the fabrication of three-layer substrate **200**, isolation trench **204** and contact holes **208** are etched through device layer **224** and sacrificial layer **222**, stopping at electrodes **206**. While shown as a single isolation trench **204** extending through both the sacrificial layer **222** and device layer **224**, the present invention is not limited thereto. For instance, an isolation trench may be formed in sacrificial layer **222**, but not device layer **224** and, likewise, an isolation trench may be formed in device layer **224**, but not sacrificial layer **222**. Or, two trenches that are not coincident may be formed in each of device layer **224** and sacrificial layer **222**.

Isolation trench **204** and contact holes **208** are lined with a dielectric **211**, such as a thermal oxide, and back-filled with conductive material, such as doped polysilicon. The doped polysilicon in contact holes **208** forms via posts **209**. In addition to providing electrical conductivity, the use of doped polysilicon also provides mechanical stiffness to micromirror structure **100**.

At this point substrate **200** is compatible with traditional CMOS circuit fabrication processes. For a typical CMOS fabrication process, the only differences between substrate **200** and normal starting material is that substrate **200** has trench isolation and comprises bonded wafers. Trench isolation and bonded wafers, however, are well-established processes in IC manufacturing. Therefore, standard processing with alignment to the trench features is preferably performed to form the integrated electronics **232**. Metal interconnects **216** and **234** are formed to connect to via posts **209** and the mirror region. At the completion of circuit formation, the substrate has a passivation layer **213** covering device layer **224**. As illustrated in figures 2e and 2f, this passivation layer is next removed from the mirror area and the mirror **210**, concentric suspension ring **214**, frame **218** and flexures are patterned and etched in device layer **224**. Mirror **210**, concentric suspension ring **214**, frame **218** and flexures are etched in device layer **224**, for example, using a deep reactive ion etch stopping on second dielectric layer **205**

Next, as shown in figure 2g, a photoresist coating **207** is applied to substrate **200** and patterned. Release holes **215** are etched through photoresist coating **207** and second dielectric **205** to expose the silicon of sacrificial layer **222**.

As illustrated in figure 2h, the silicon of sacrificial layer **222** bound by first dielectric layer **203**, second dielectric layer **205** and the dielectric lining isolation trench **204** is then isotropically etched through release holes **215** using, for example, a Xenon Diflouride ($XeF_2$) dry etch. Etching sacrificial layer **222** forms a cavity **217** underneath mirror **210**, concentric suspension ring **214**, frame **218** and the flexures. Formation of cavity **217** releases mirror **210**, concentric suspension ring **214**, frame **218** and the flexures for movement.

Referring to figures 2i and 2j, the dielectric in cavity **217** is next removed by, for example, an oxide etch using Hydroflouric Acid (HF). This is followed by an oxygen plasma resist strip to remove photoresist coating **207**, which results in the structure as shown in figure 2j. Finally, a layer of reflective material, preferably gold, is deposited and patterned on mirror **210** to complete the structure as shown in figure 1c.

While it is preferable to place the coating on mirror **210** as the last step in fabrication, the reflective material can be deposited and etched on mirror **210** or mirror region during other times of the fabrication process. For instance, the reflective material can be placed on the mirror region of device layer **224** prior to the etching of mirror **210**, concentric suspension ring **214** and frame **218** and flexures. In this case, after circuit fabrication, part of passivation layer **213** is removed above the mirror region. A thin layer of reflective material, preferably gold, is deposited and patterned on the mirror region. Next, mirror **210**, concentric suspension ring **214** and frame **218** and flexures are patterned and etched in device layer **224**. The rest of the fabrication continues as previously described to the formation of cavity **217** and the corresponding oxide etch and photoresist strip.

Figure 3 illustrates another embodiment of a micromirror structure **300** constructed according to the principles of the present invention. In the embodiment of figure 3, polycrystalline silicon ("polysilicon") is used as a device layer **324** instead of single crystal silicon. It should be noted that using polysilicon to form a micromirror will increase mirror roughness while reducing compatibility with standard CMOS fabrication. Polysilicon also increases mirror curvature because of stress gradients in the polysilicon. However, the use of polysilicon is advantageous at times because

using polysilicon decreases the cost of fabricating the device.

As described, micromirror structure **300** is similar to micromirror structure **100**. Micromirror structure **300** is formed from a substrate having a handle layer **320**, a sacrificial layer **322** and device layer **324**. Handle layer is separated from sacrificial layer **322** by a first dielectric **303**, such as silicon dioxide. Polysilicon device layer **324** is separated from sacrificial layer **322** by a second dielectric **305**, such as silicon dioxide. Handle layer **320** and sacrificial layer **322** comprise single crystal silicon, while, as described above, device layer **324** comprises polysilicon.

As illustrated, a mirror **310** formed from polysilicon device layer **324** is suspended over a cavity created by the removal of sacrificial layer **322** underlying mirror **310**. Mirror **310** has a coating **330** thereon to increase the reflectivity. As with mirror **110**, mirror **310** is preferably connected to a concentric suspension ring **314** via a first set of flexures and concentric suspension ring **314** is connected to a frame **318** via a second set of orthogonally oriented flexures. An isolation trench **304** extends down to handle layer **320** through sacrificial layer **322** and surrounds the area containing mirror **310** and associated frame **318**. Isolation trench **304** is partially formed from a conductive material, such as doped polysilicon.

Similar to isolation trench **304**, via posts **309**, filled with a conductive material such as doped polysilicon, extend down through sacrificial layer **322**. Via posts **309** connect to interconnects **306** formed on handle layer **320**. Electrical interconnections **316** and **334** are formed on top of the device layer to apply the appropriate actuation voltages.

Fabrication of micromirror structure **300** is similar to the fabrication of micromirror structure **100**. Referring to figures 4a, 4b, 4c and 4d, the fabrication process for micromirror structure **300** begins with interconnects and actuation electrodes **406** formed on a single crystal silicon wafer **420**. Interconnects and actuation electrodes **406** illustrated are formed using patterned deposits of polysilicon. However, as described above, other manners of forming interconnects and actuation electrodes **406**, such as patterned diffusions into silicon wafer **420**, are possible. A single crystal wafer **422** is bonded to wafer **420** using wafer bonding. Wafer **422** is ground to the desired sacrificial layer thickness using, for example, a combination of mechanical and chemical-mechanical polishing (CMP). Alternative techniques, similar to those described above may also be used to form two-layer substrate **400**.

Next, isolation trench **404** and via holes **408** are etched through wafer **422**, stopping at interconnects **406**. A dielectric, such as a thermal oxide, is grown on top of

wafer **422** forming dielectric layer **405** and on the walls of isolation trench **404** and via holes **408** forming linings **411**. Anchor holes **421**, which will be used provide support to the mirror, are patterned and etched in dielectric layer **405**.

As illustrated in figure 4e, a device layer **424** and via posts **409** are formed and isolation trenches are filled from polysilicon deposition on top of second dielectric layer **405**. Polysilicon forming the device layer is deposited to the desired device thickness. As shown in figure 4f, device layer **424** is then etched to form interconnect features **419** and anchor features **423**.

A pre-metal dielectric deposition and contact etch is next performed, followed by a metal deposition and etch step and a passivation deposition step. As shown in figure 4g, these steps form metal interconnects **416** and **434** covered by a passivation layer **413**.

As illustrated in figures 4h and 4i, this passivation layer is next removed from the mirror area and the mirror **410**, concentric suspension ring **414**, frame **418** and flexures are patterned and etched in device layer **424**. Mirror **410**, concentric suspension ring **414**, frame **418** and flexures are etched in device layer **424**, for example, using a deep reactive ion etch stopping on second dielectric layer **405**.

Next, as shown in figure 4j, a photoresist coating **407** is applied to substrate **400** and patterned. Release holes **415** are etched through photoresist coating **407** and second dielectric **405** to expose the silicon of sacrificial layer **422**.

As illustrated in figure 4k, the silicon of sacrificial layer **422** bound by first dielectric layer **403**, second dielectric layer **405** and the dielectric lining isolation trench **404** is then isotropically etched through release holes **415** using, for example, a Xenon Diflouride ($XeF_2$) dry etch. Etching sacrificial layer **422** forms a cavity **417** underneath mirror **410**, frame **418** and the flexures. Formation of cavity **417** releases mirror **410** and the flexures for movement.

As illustrated in figure 4l, the dielectric in cavity **417** is next removed by, for example, an oxide etch using hydrofluoric acid (HF). This is followed by an oxygen plasma resist strip to remove photoresist coating **407** to complete the structure as shown in figure 4m. Finally, a layer of reflective material, preferably gold, is deposited and patterned on mirror **410** to complete the structure shown in figure 3.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

## CLAIMS

1. A method of fabricating a microelectromechanical system, said method comprising:

providing a substrate comprising a handle layer of silicon, a device layer of silicon and a sacrificial layer of silicon disposed between said handle layer and said device layer;

forming a micromechanical structure in said device layer; and

removing at least a portion of said sacrificial layer of silicon underlying said micromechanical structure to release said micromechanical structure for movement

2. A method of fabricating a microelectromechanical system, as per claim 1, wherein said silicon of said sacrificial layer is single crystal silicon.

3. A method of fabricating a microelectromechanical system,as per claim 1, wherein said forming step further comprises:

forming an isolation trench that extends through at least said device layer.

4. A method of fabricating a microelectromechanical system, as per claim 1, wherein said handle layer is separated from said sacrificial layer by a first dielectric layer, said sacrificial layer is separated from said device layer by a second dielectric layer, and said forming step further comprises:

forming an isolation trench that extends through at least said sacrificial layer, said isolation trench defining a release area in said sacrificial layer; and

etching said silicon of said device layer to form said micromechanical structure

5. A method of fabricating a microelectromechanical system, as per claim 4, wherein said silicon of said device layer is polysilicon.

6. A method of fabricating a microelectromechanical system, as per claim 4, wherein said silicon of said device layer is single crystal silicon.

7. A method of fabricating a microelectromechanical system, as per claim 4,

wherein said isolation trench additionally extends through said device layer.

8. A method of fabricating a microelectromechanical system, as per claim 4, said removing step further comprising:

placing a photoresist layer on top of said device layer over at least said micromechanical structure;

forming release etch holes through said photoresist layer and said second dielectric layer; and

etching said sacrificial layer of silicon underlying said micromechanical structure.

9. A method of fabricating a microelectromechanical system, as per claim 8, wherein said first dielectric layer is used as an etch stop for said etching of said sacrificial layer.

10. A method of fabricating a microelectromechanical system, as per claim 8, wherein said second dielectric layer is used as an etch stop for said etching of said sacrificial layer.

11. A method of fabricating a microelectromechanical system, as per claim 8, wherein said isolation trench is used as an etch stop for said etching of said sacrificial layer.

12. A method of fabricating a microelectromechanical system, as per claim 4, wherein said handle layer has actuation electrodes formed thereon.

13. A method of fabricating a microelectromechanical system, as per claim 12, said forming step further comprising:

forming via posts extending through at least said sacrificial layer to contact said actuation electrodes.

14. A method of fabricating a microelectromechanical system, as per claim 13, wherein said via posts additionally extend through said device layer.

15. A method of fabricating a microelectromechanical system, as per claim 4, wherein actuation electrodes are formed on the bottom of said sacrificial layer.

16. A method of fabricating a microelectromechanical system, as per claim 1, said method further comprising:

bonding a silicon-on-insulator wafer to a handle wafer of silicon to create said substrate.

17. A method of fabricating a microelectromechanical system, as per claim 1, said method further comprising:

bonding a first silicon-on-insulator wafer to a handle wafer of silicon and removing a handle layer of said first silicon on insulator wafer to create said sacrificial layer; and

bonding a second silicon on insulator wafer to said sacrificial layer and removing a handle layer of said second silicon on insulator wafer to create said device layer.

18. A method of fabricating a microelectromechanical system, as per claim 1, said method further comprising:

bonding a first wafer of silicon to a second wafer of silicon;

bonding a third wafer of silicon to said first wafer of silicon; and

whereby said substrate is created.

19. A method of fabricating a microelectromechanical system, as per claim 1, wherein said micromechanical structure is any one of: a micro-optical device, an inertial sensor, or an actuator.

20. A method of fabricating a microelectromechanical system, as per claim 19, wherein said micro-optical device is a micromirror.

21. A method of releasing a micromechanical structure for movement, said micromechanical structure etched in a silicon device layer, said method comprising:

etching a silicon sacrificial layer disposed between said micromechanical structure and a silicon handle layer.

22. A method of releasing a micromechanical structure for movement, as per claim 21, wherein said micromechanical structure is a micromirror.

23. A microfabricated device comprising:

a substrate having a device layer;

a least one micro-optical device etched on said device layer and released for movement by removal of an underlying sacrificial layer of silicon; and

active electronics formed on said device layer.

24. A microfabricated device as per claim 23, wherein said micro-optical device is a micromirror.

25. A microfabricated device as per claim 23, wherein said active electronics are formed via CMOS fabrication techniques.

26. A microfabricated device as per claim 23, wherein said silicon of said device layer is single crystal silicon.

27. A microelectromechanical device comprising:

a handle layer of silicon having actuation electrodes formed thereon;

a device layer of silicon having a micromechanical structure formed thereon; and

a sacrificial layer of silicon disposed between said handle layer and said device layer of silicon, said sacrificial layer of silicon having a portion underlying said micromechanical structure removed to form an actuation cavity below said micromechanical structure.

28. A microelectromechanical device as per claim 27, further comprising:

at least one isolation trench extending through said device layer and said sacrificial layer and enclosing said cavity and micromechanical structure.

29. A microelectromechanical device as per claim 28, wherein said isolation trench is lined with a dielectric and filled with a conductive material.

30. A microelectromechanical device as per claim 29, wherein said dielectric is an oxide and said conductive material is doped polysilicon.

31. A microelectromechanical device as per claim 27, further comprising:

at least one via post extending through said device and said sacrificial

layer for electrical connection to said actuation electrodes.

32. A microelectromechanical device as per claim 27, wherein said silicon of said device layer is polysilicon.

33. A microelectromechanical device as per claim 27, wherein said silicon of said device layer is single crystal silicon.

34. A microelectromechanical device as per claim 33, said device further comprising:

integrated electronics formed on said device layer.

35. A microelectromechanical device as per claim 34, wherein said integrated electronics electrically connected to said actuation electrodes by at least one via post extending through said device layer and said sacrificial layer.

36. A microelectromechanical device as per claim 27, wherein said micromechanical structure is a micromirror.

37. A micromirror device comprising:

a substrate having a device layer, a handle layer and a sacrificial layer made of silicon disposed between said device layer and said handle layer;

an isolation trench extending through said device layer and said sacrificial layer, said isolation trench defining a mirror region and electrically isolating said mirror region;

a mirror formed from said device layer in said mirror region above actuation electrodes formed on said handle layer; and

a cavity formed below said mirror by removing a portion of said sacrificial layer of silicon.

38. A micromirror device as per claim 37, wherein said device layer is single crystal silicon

39. A micromirror device as per claim 38, said micromirror device further comprising:

active electronics formed on said substrate in said device layer.

40. A micromirror device as per claim 39, wherein said active electronics are connected to said actuation electrodes through a via post extending through said device layer and said sacrificial layer.

41. A micromirror device as per claim 37, wherein said mirror comprises:

a central mirror plate;

a concentric suspension ring connected to said central mirror plate;

a frame formed from said device layer in said mirror region; and

wherein said mirror is connected to said frame via flexures, said flexures comprise a first set of flexures connected between said central mirror plate and said concentric suspension ring and a second set of orthogonally oriented flexures connected between said concentric suspension ring and said frame.

42. A micromirror device as per claim 41, wherein said central mirror plate has a coating of reflective material thereon.

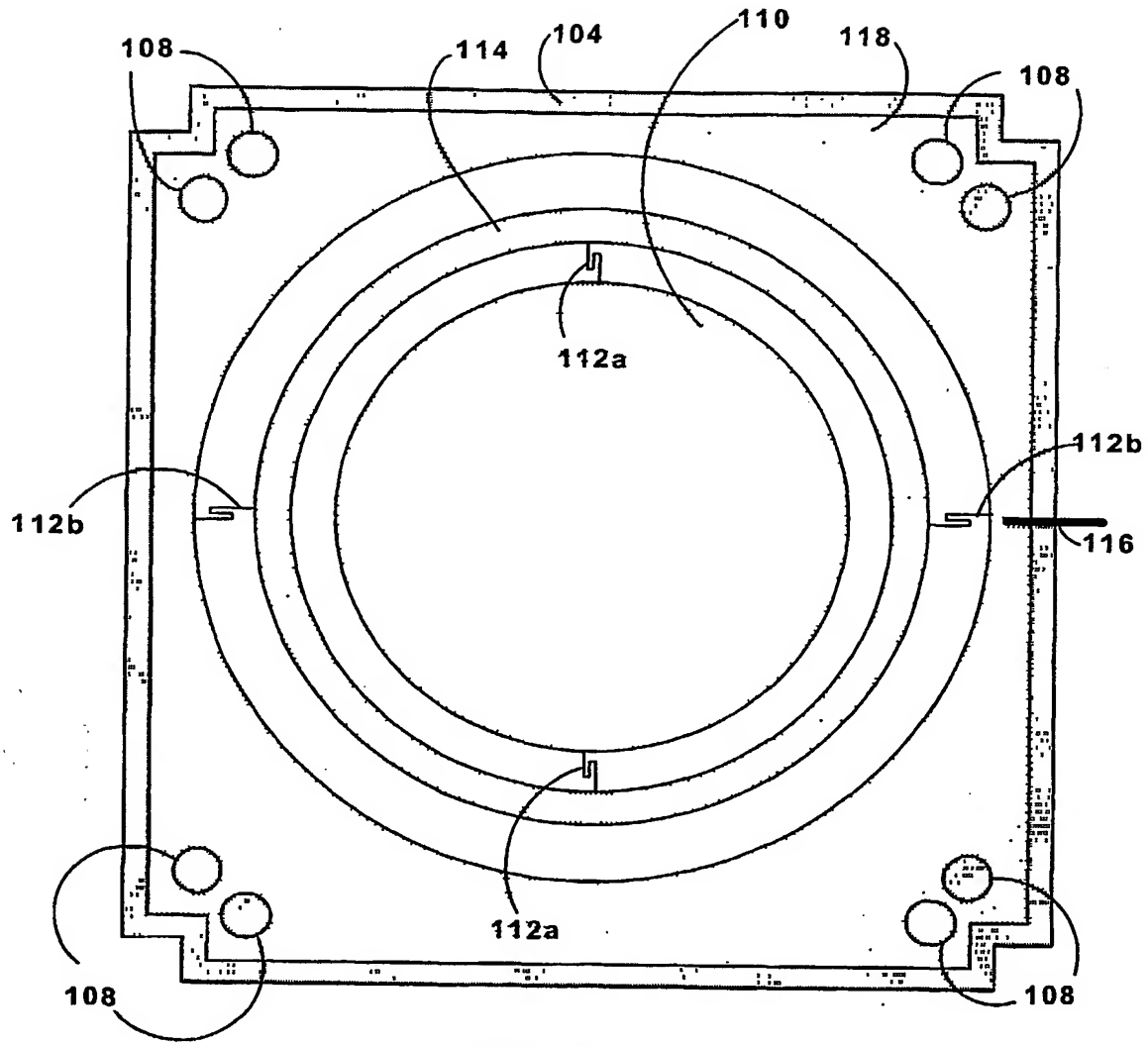


Figure 1a

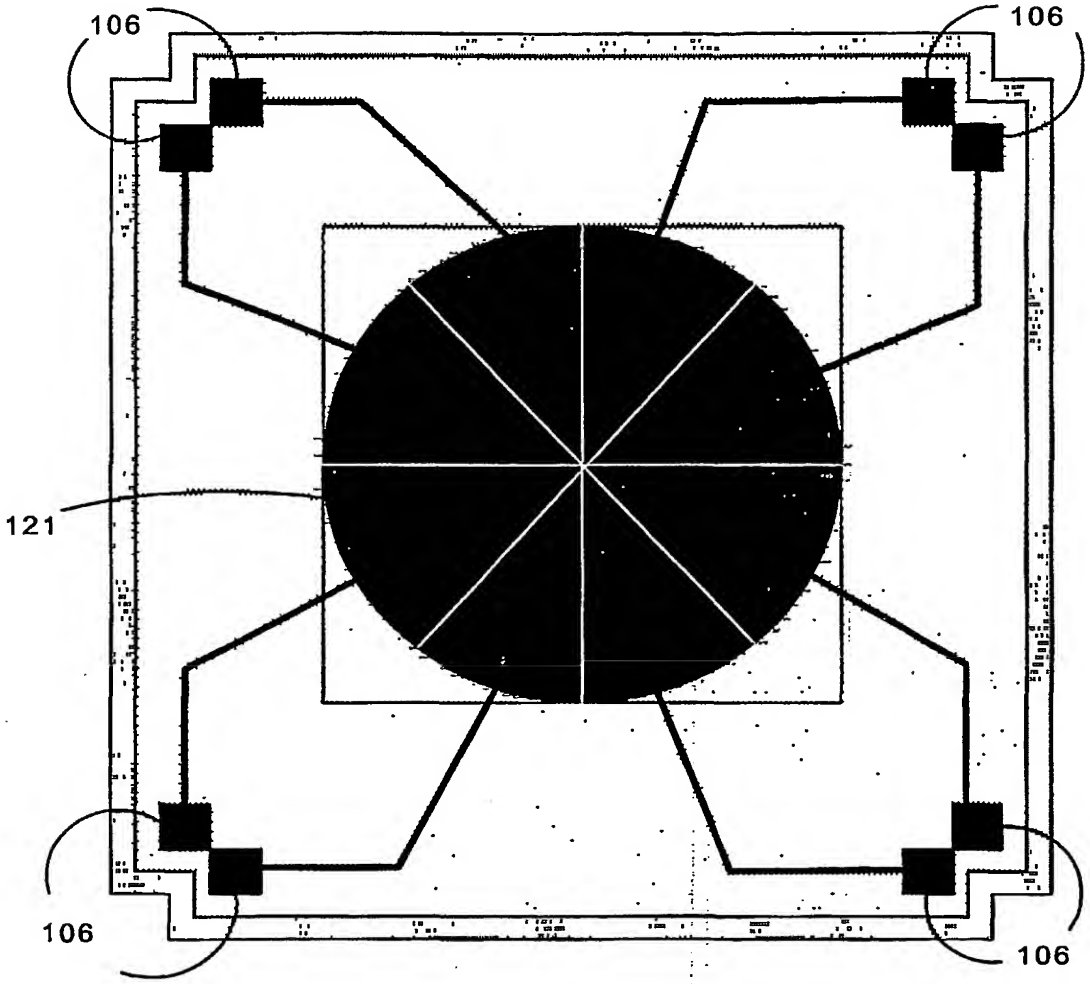


Figure 1b

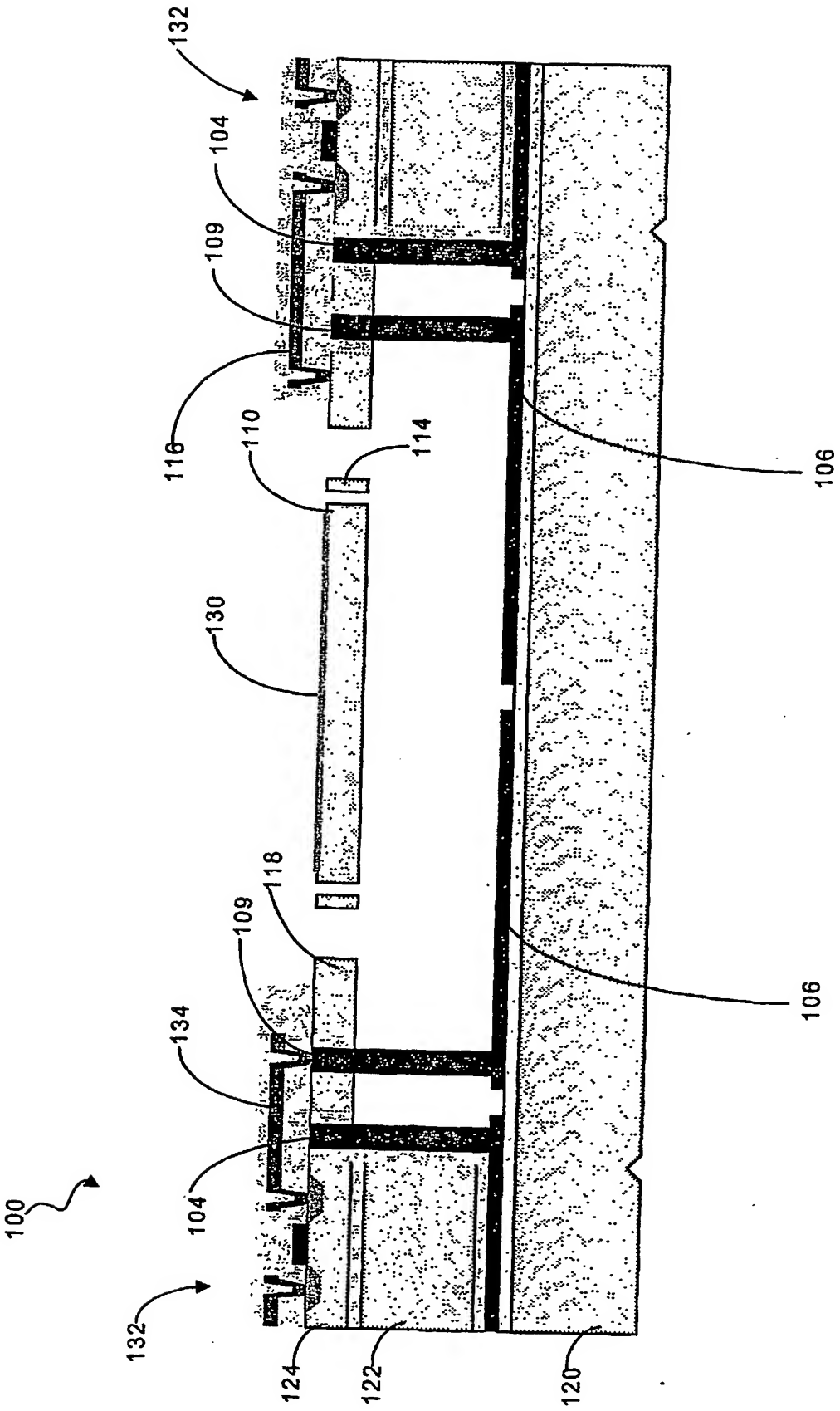
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Figure 1c

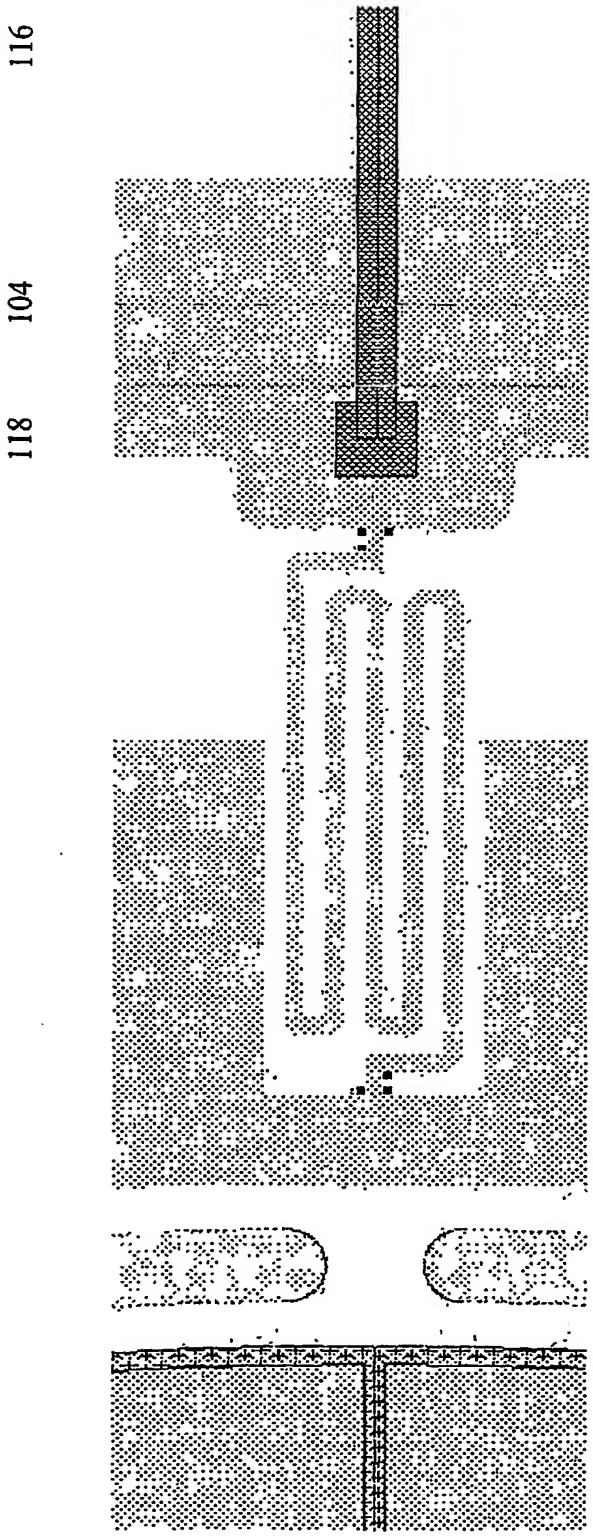


Figure 1d

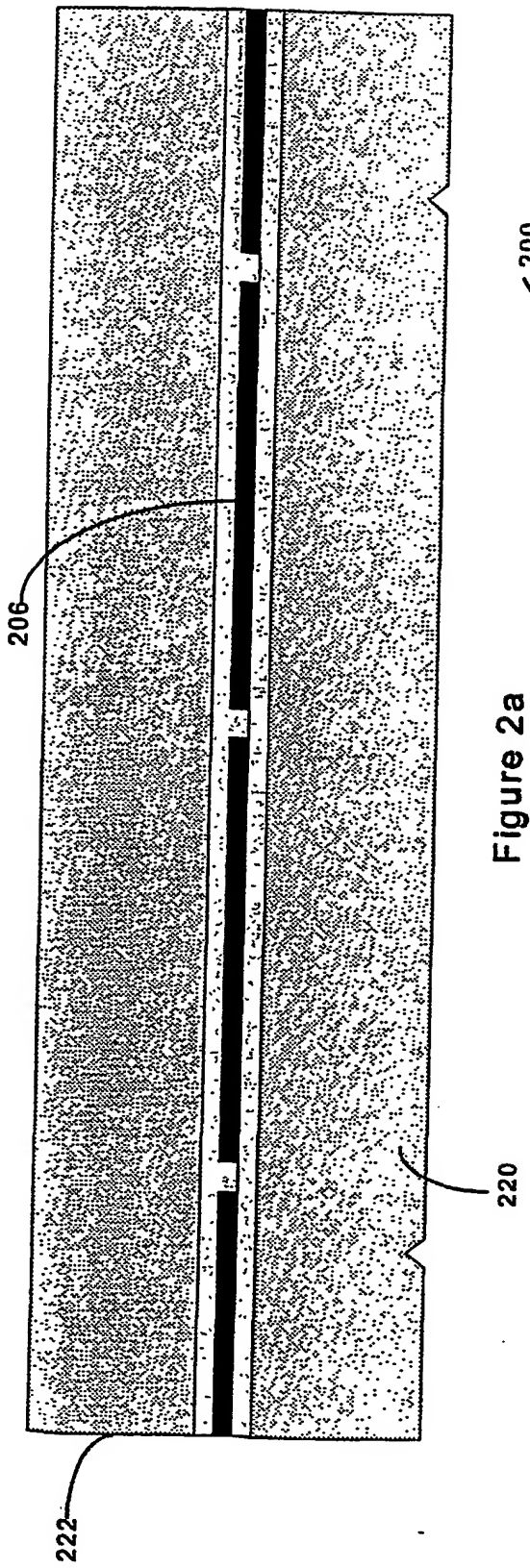


Figure 2a

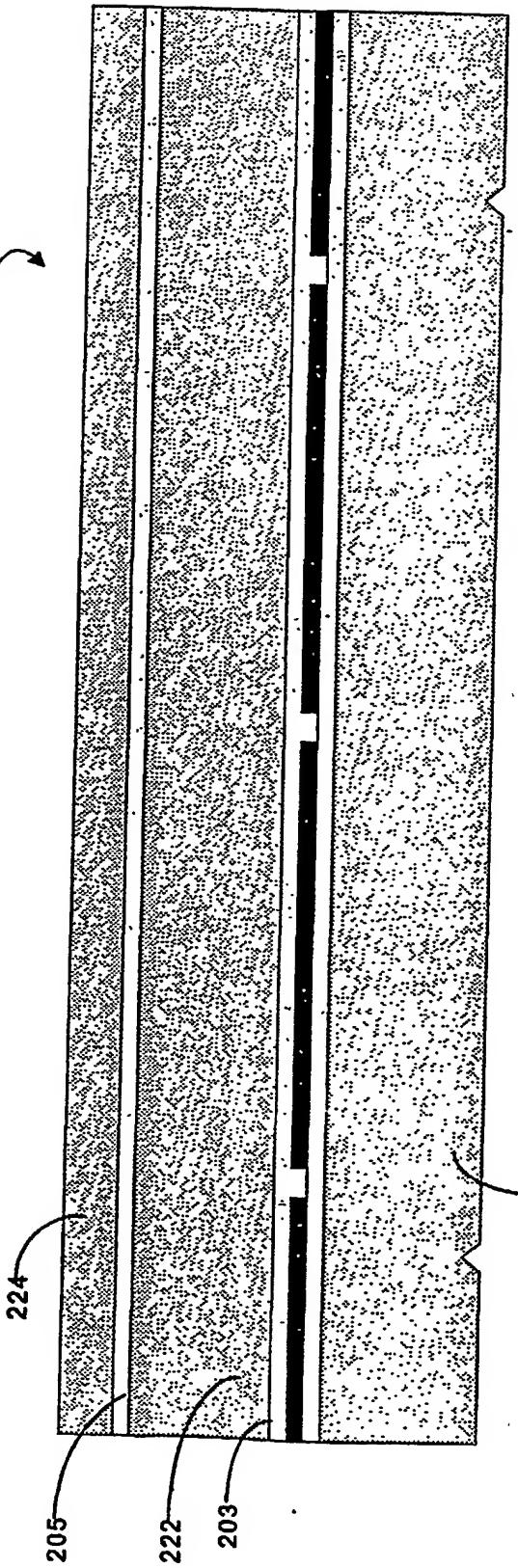


Figure 2b

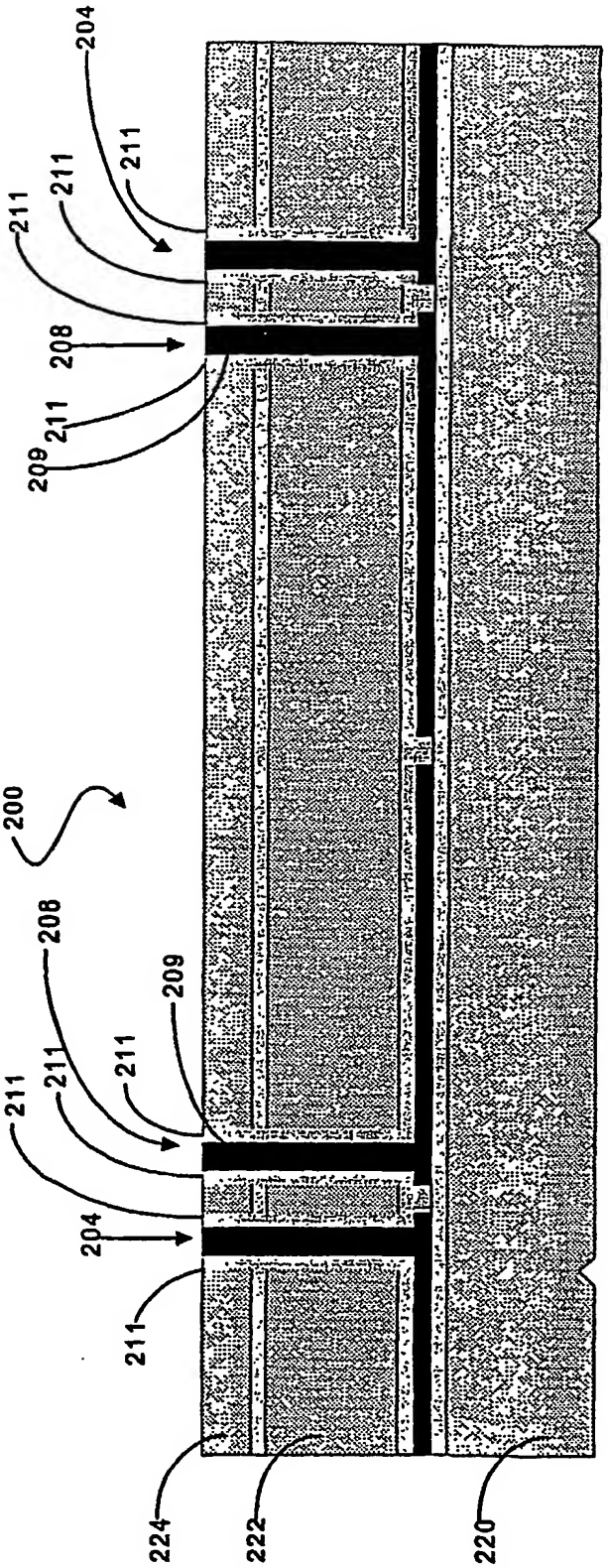


Figure 2c

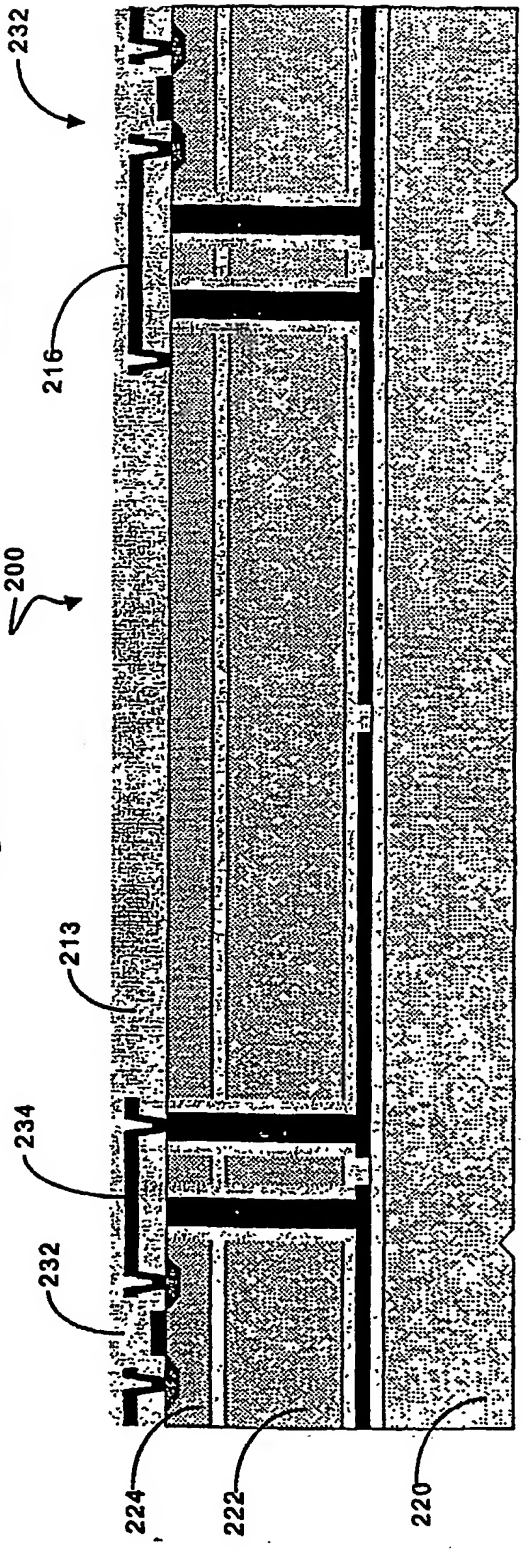


Figure 2d

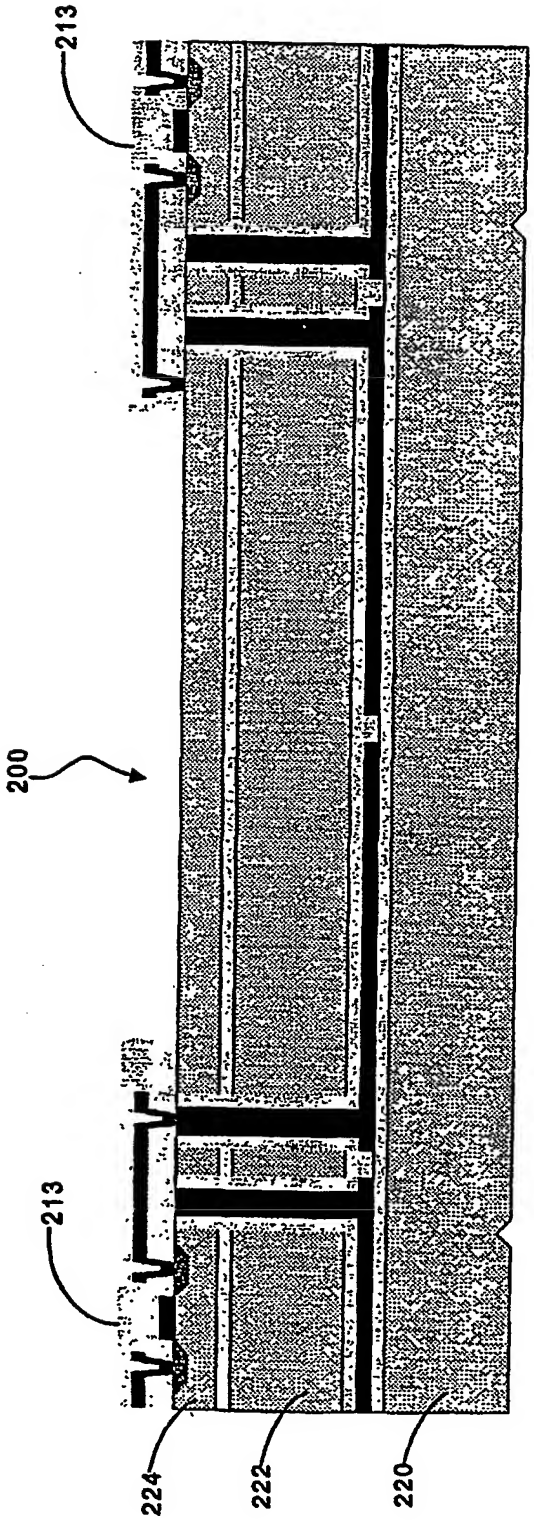


Figure 2e

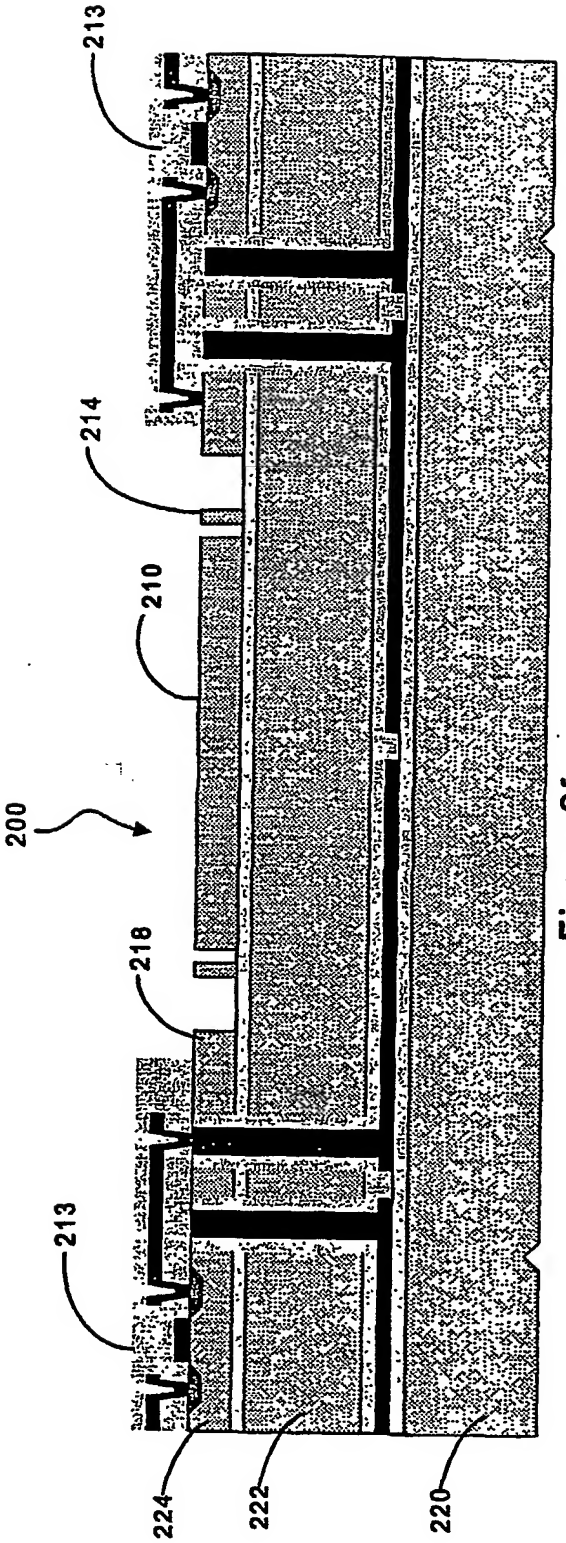


Figure 2f

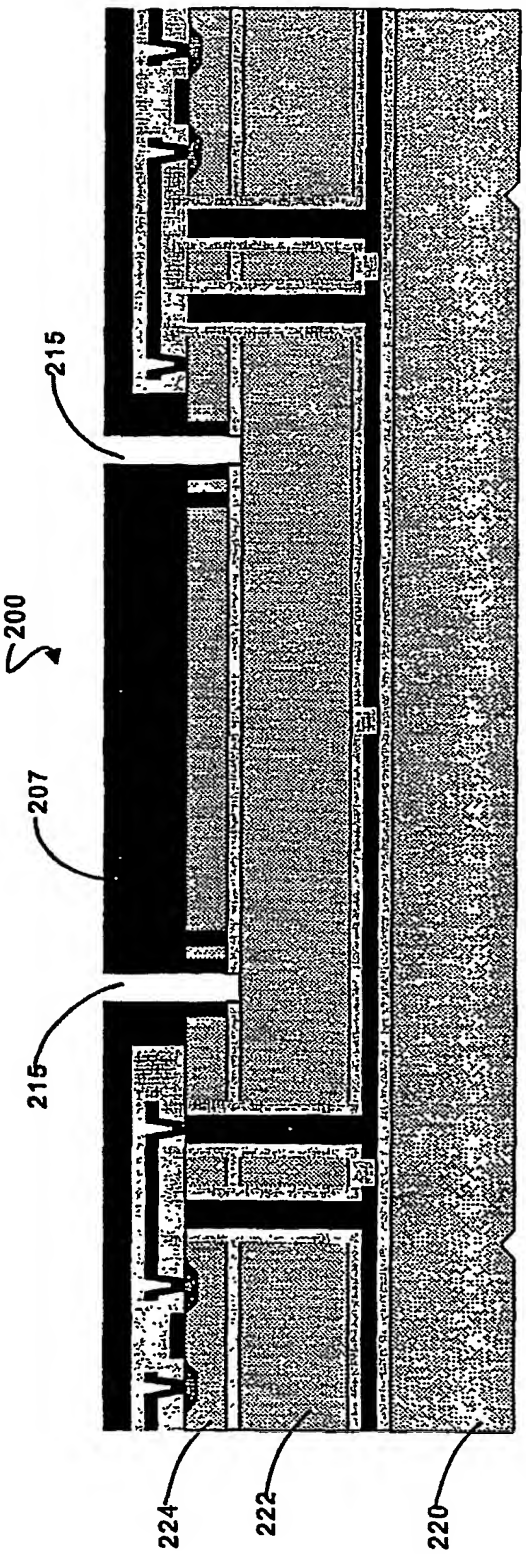


Figure 2g

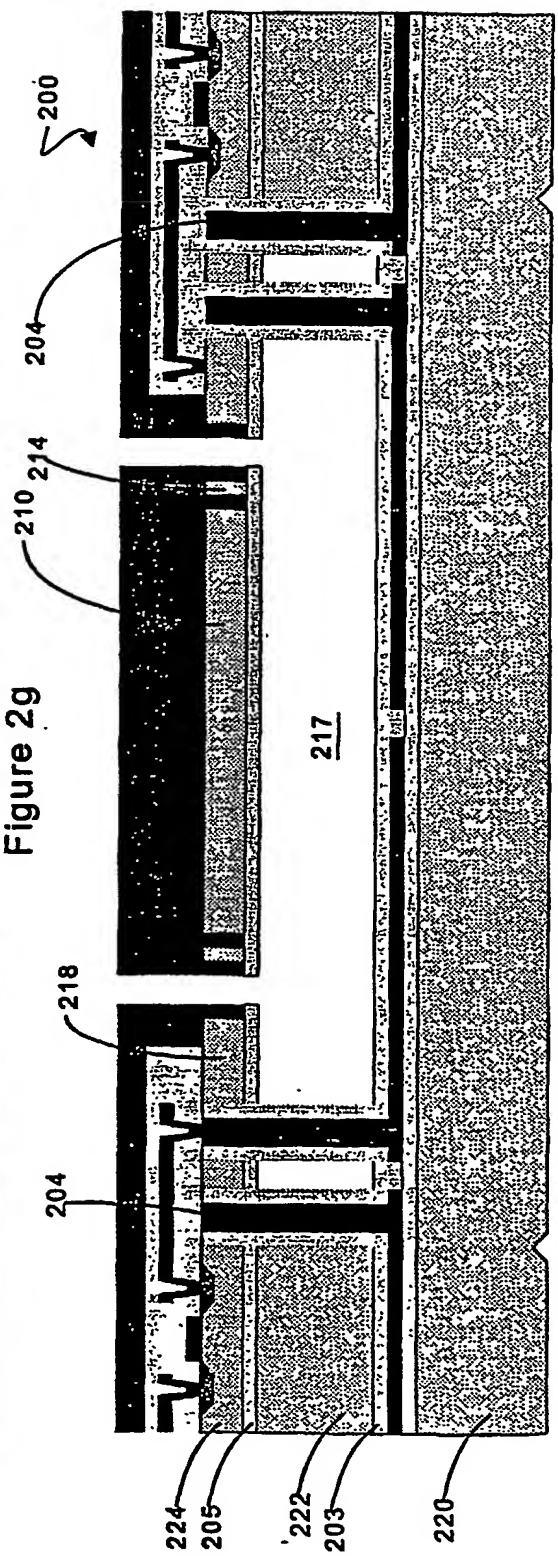


Figure 2h

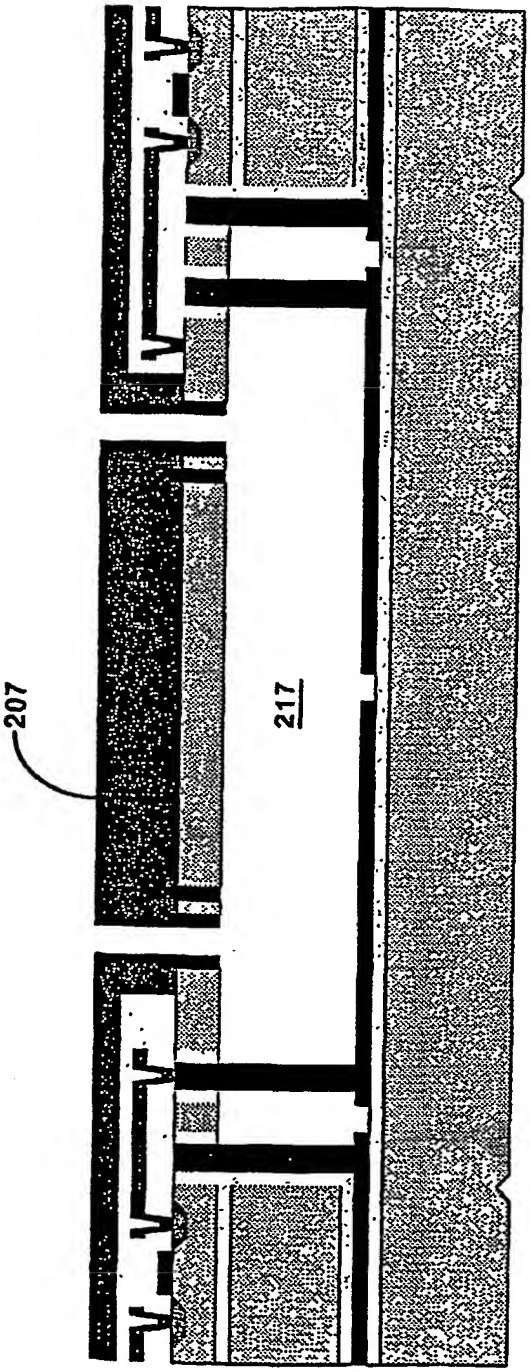


Figure 2i

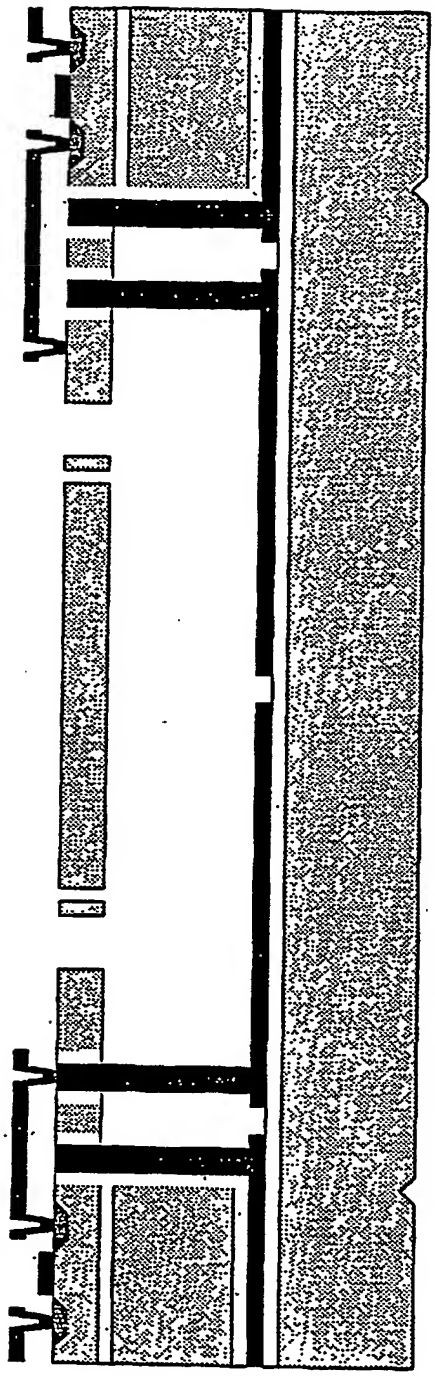

Figure 2j

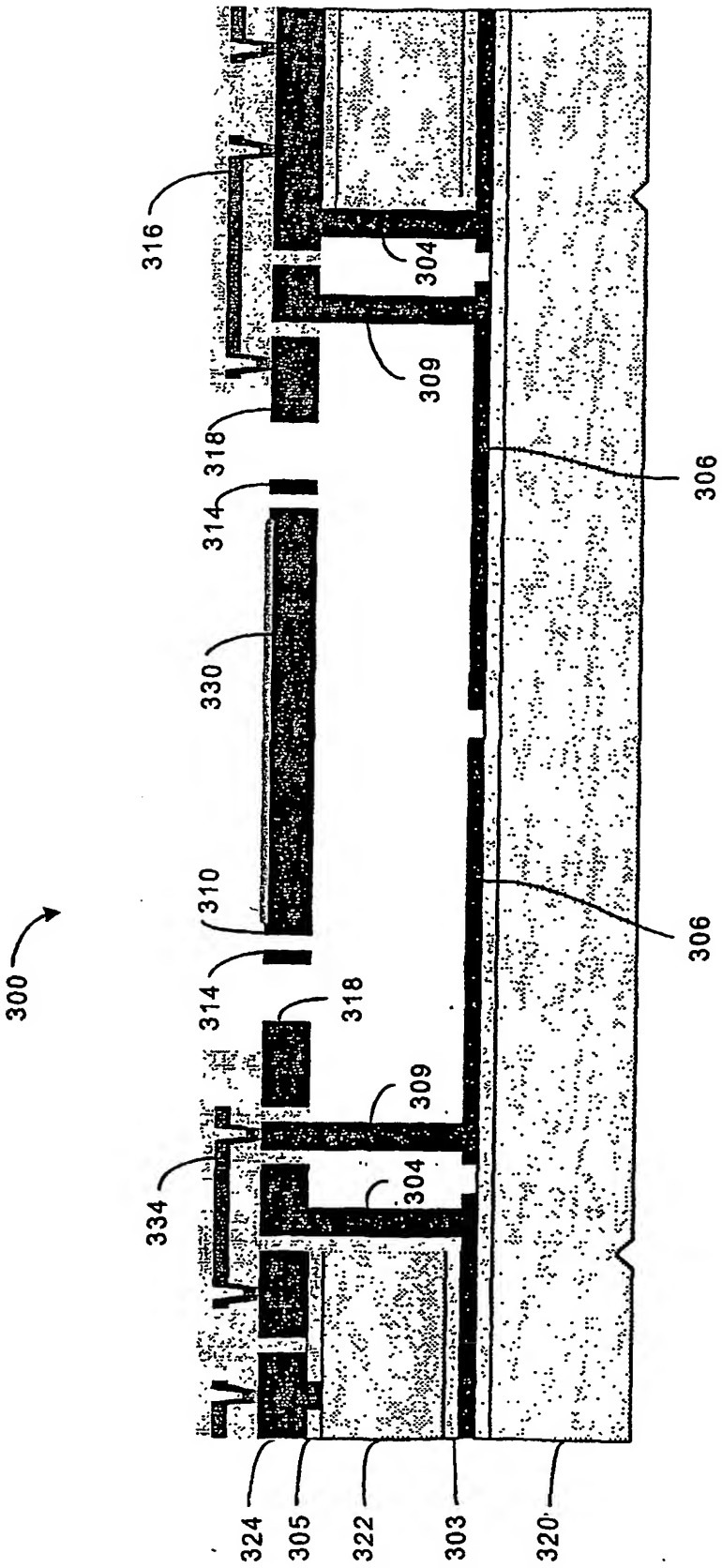
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Figure 3

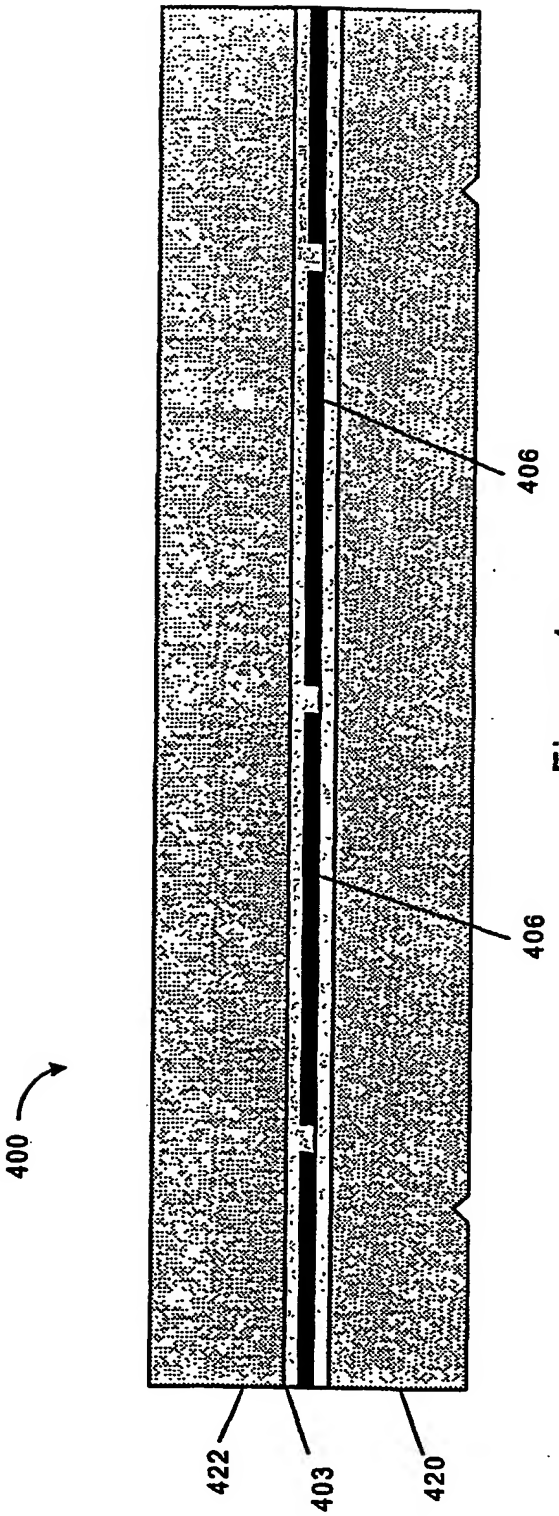


Figure 4a

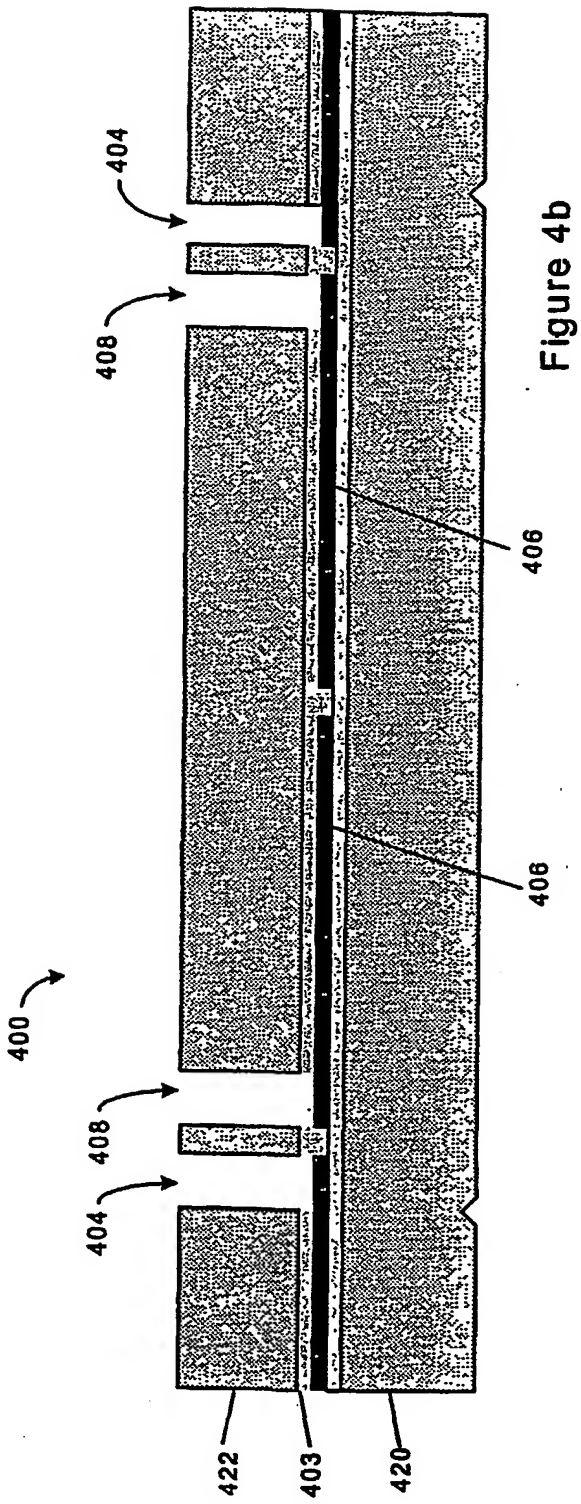


Figure 4b

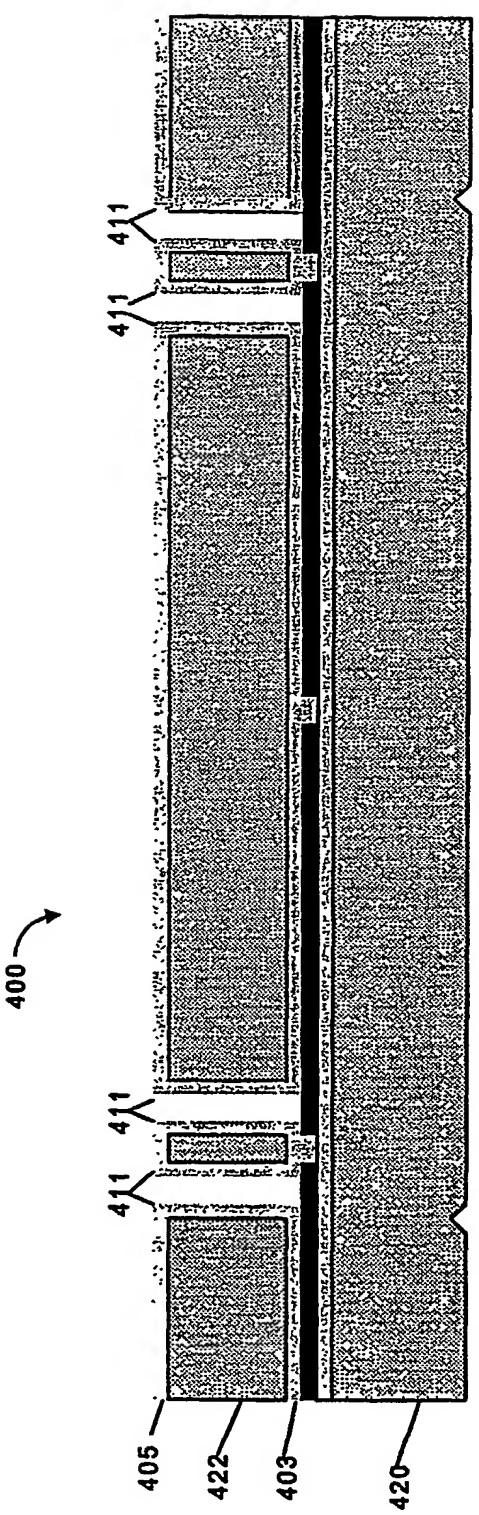


Figure 4c

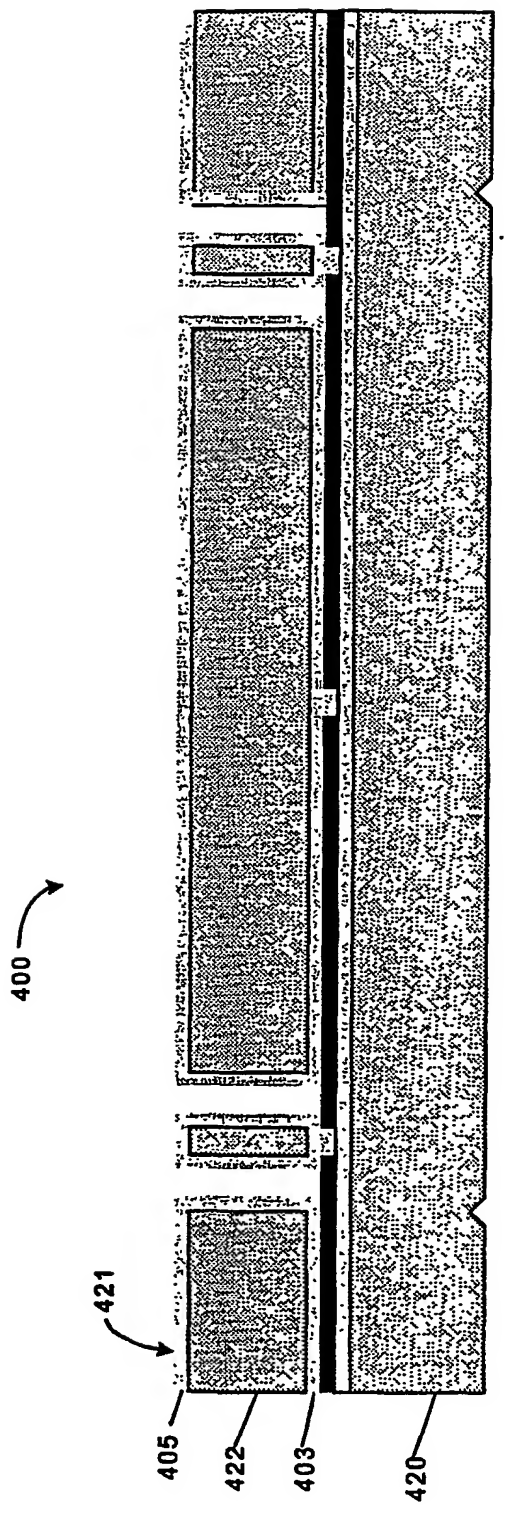


Figure 4d

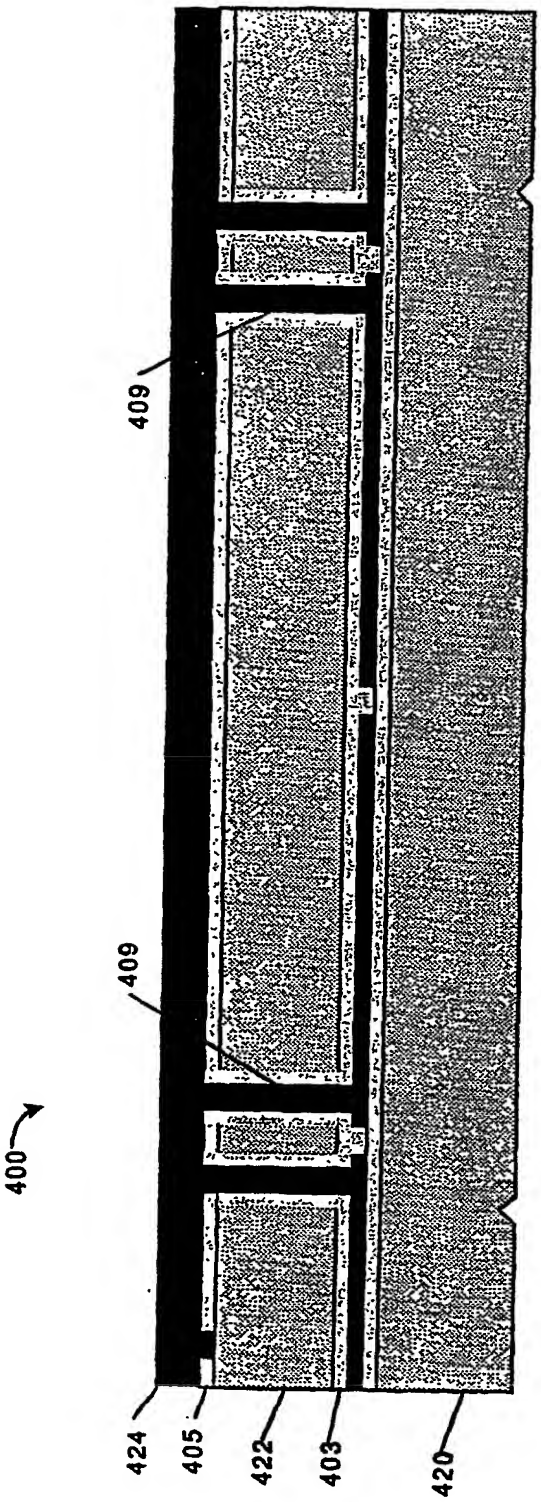


Figure 4e

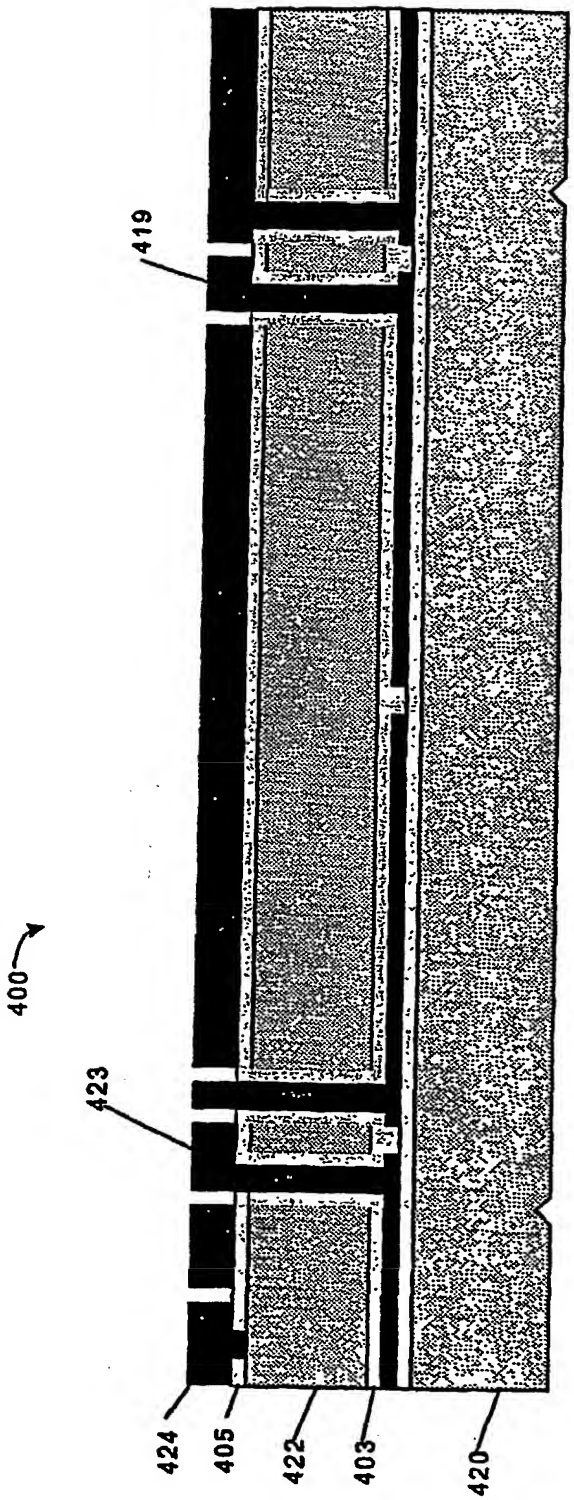


Figure 4f

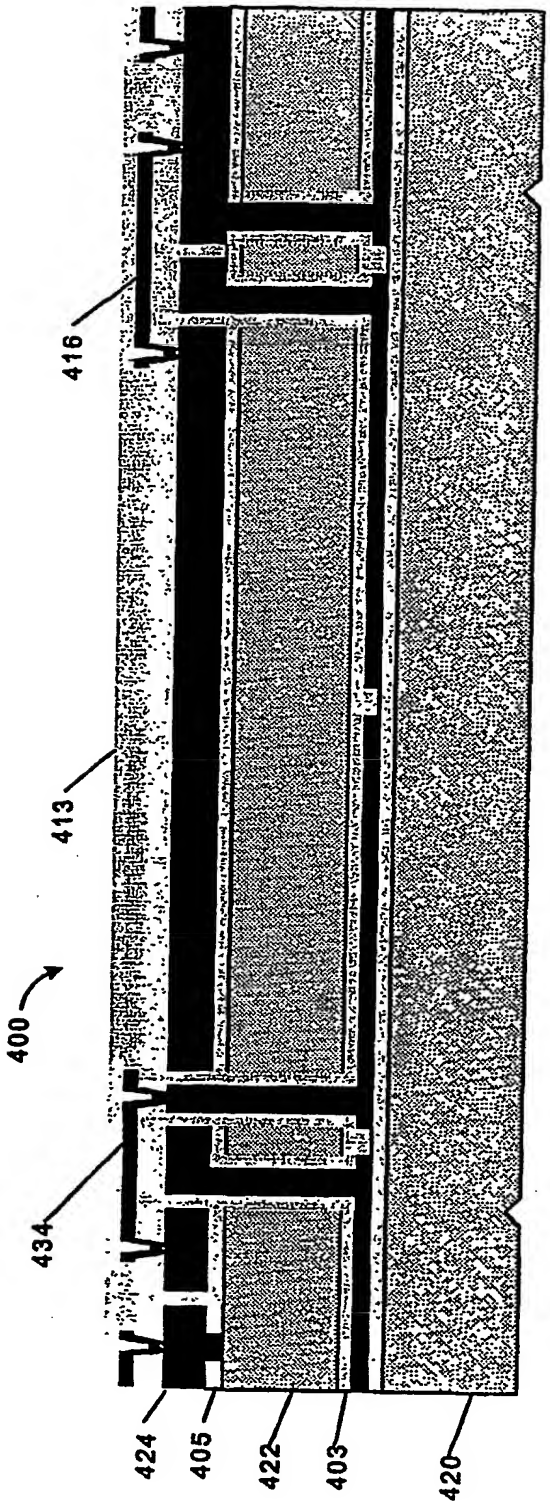


Figure 4g

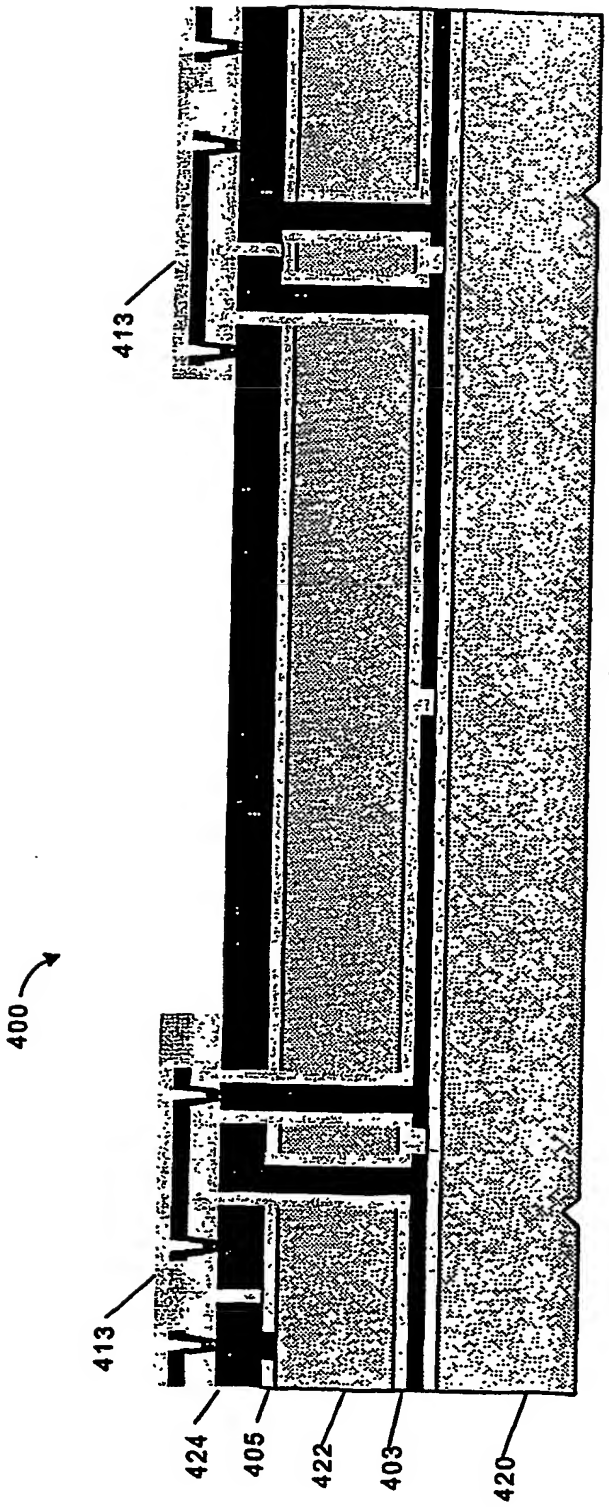


Figure 4h

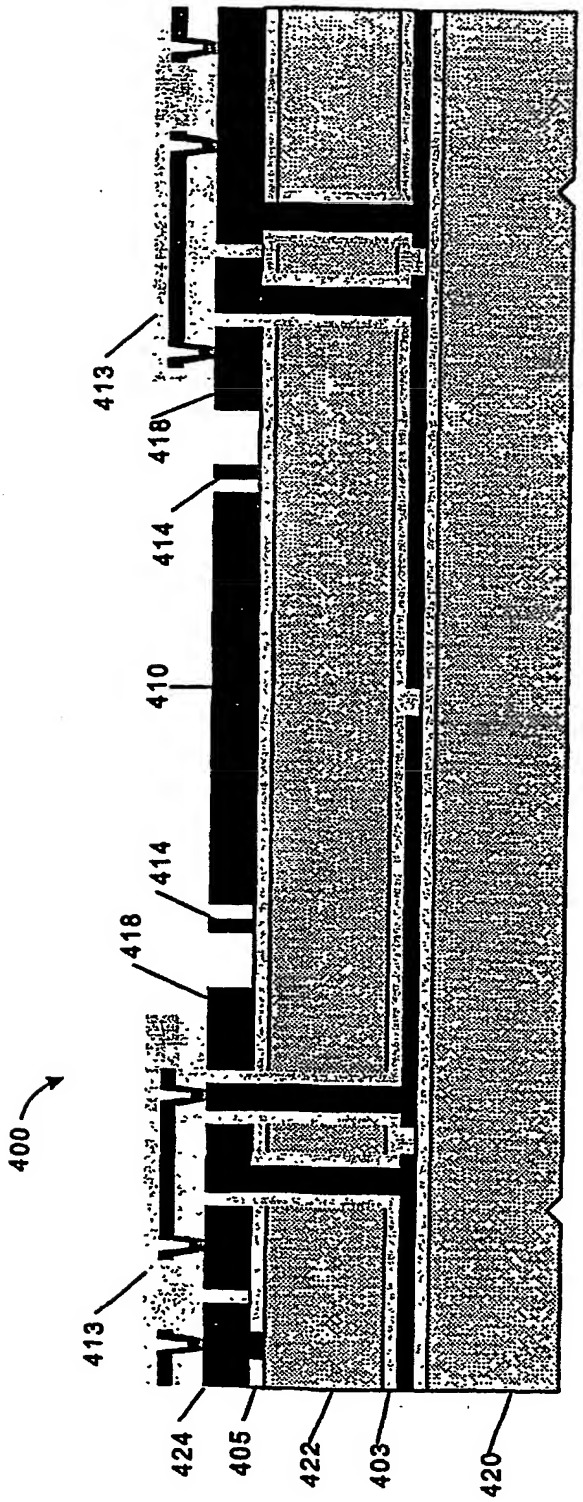


Figure 4i

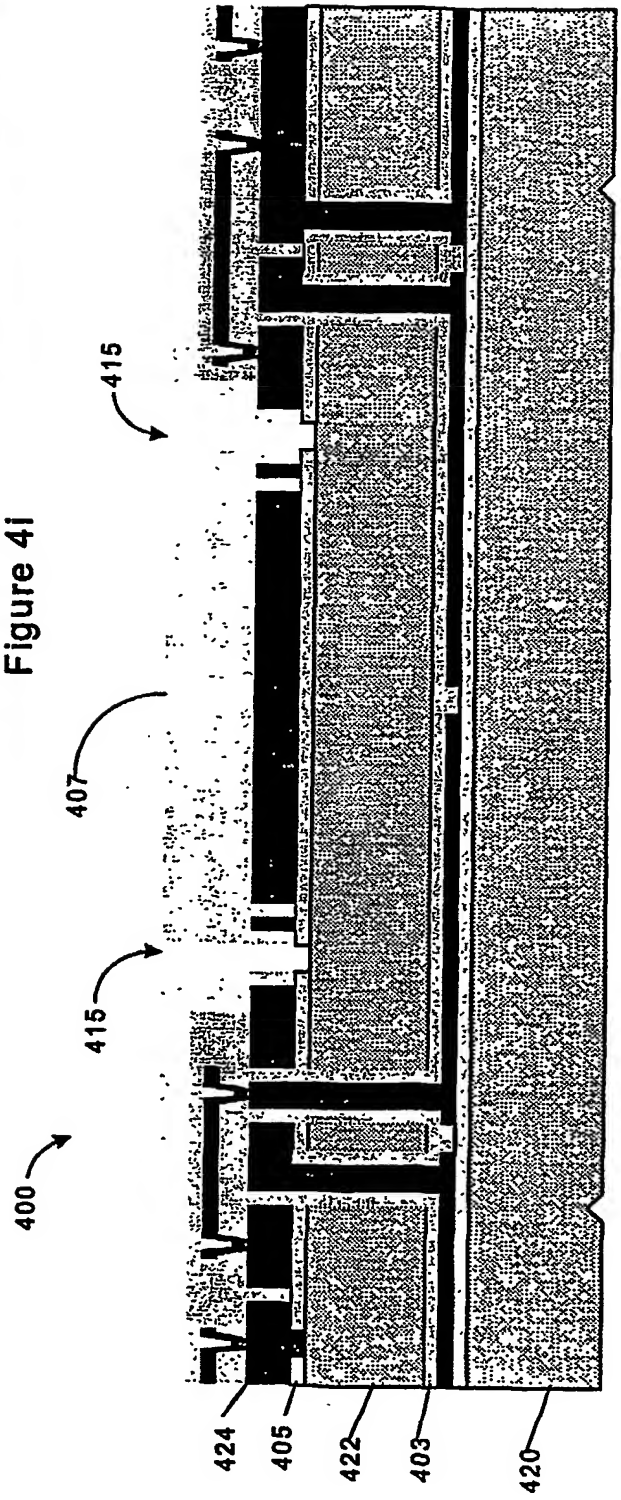


Figure 4j

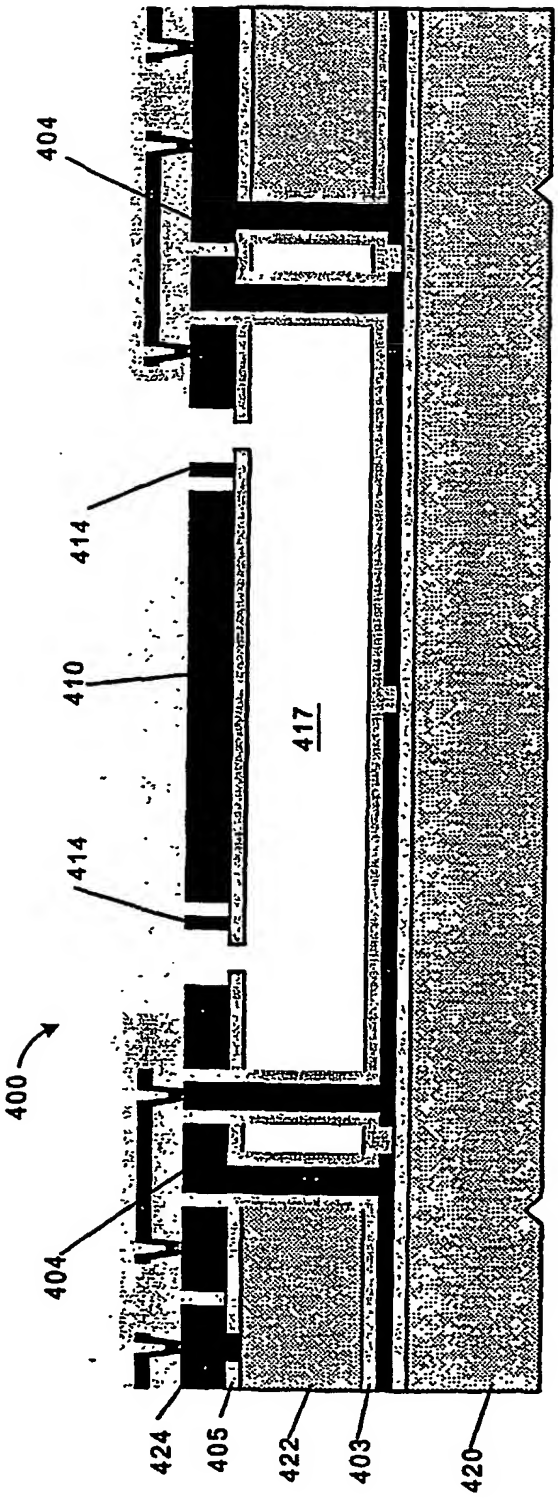


Figure 4k

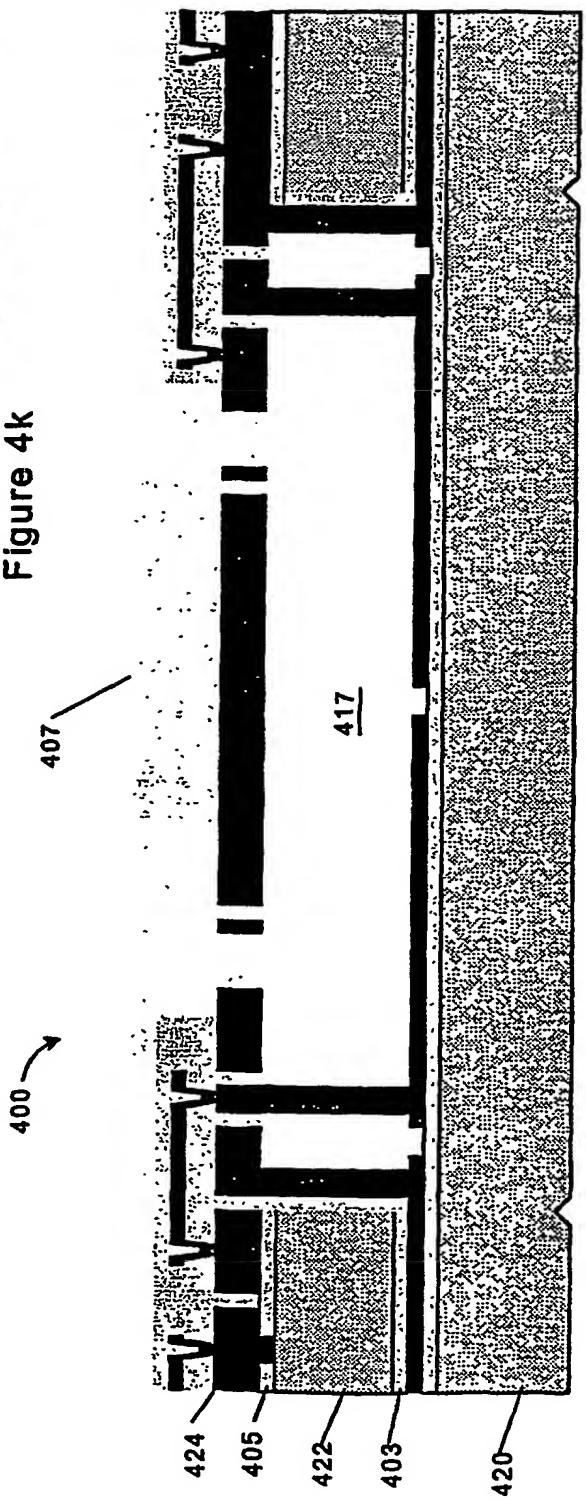


Figure 4l

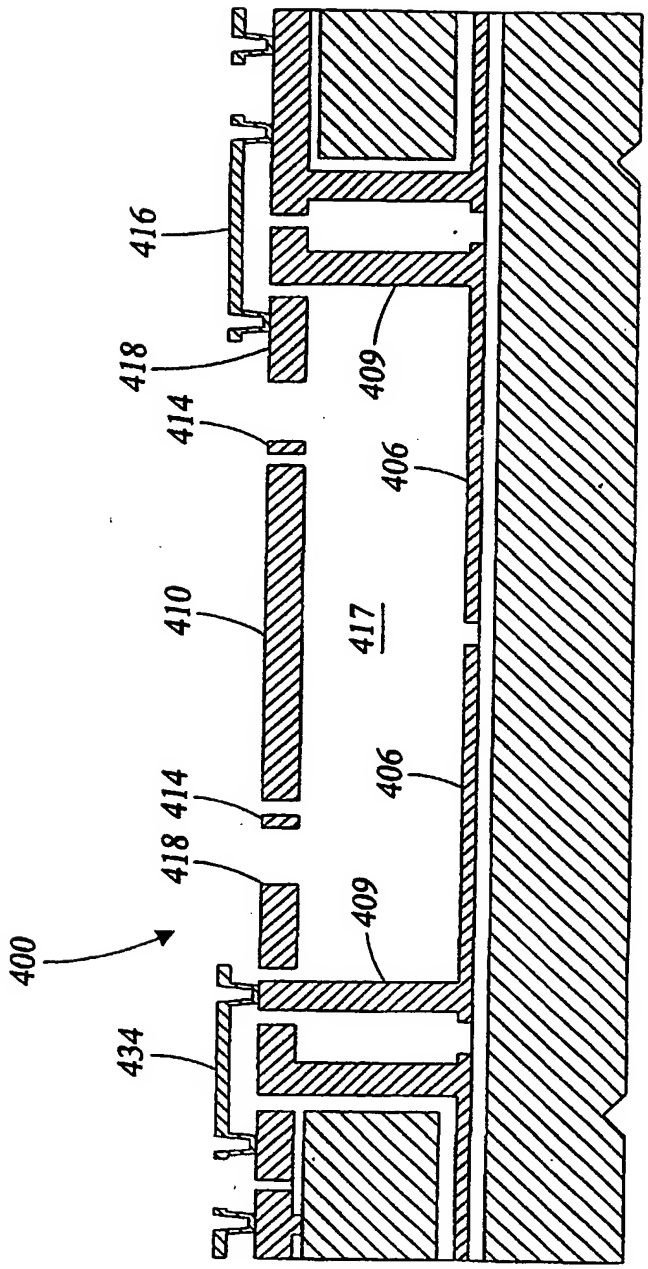


FIG. 4m

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(22) International Filing Date: 3 August 2001 (03.08.2001)

(25) Filing Language: English

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60/222,751 3 August 2000 (03.08.2000) US

(71) Applicant: ANALOG DEVICES, INC. [US/US]; One Technology Way, Norwood, MA 02062-9106 (US).

(72) Inventors: BROSNIHAN, Timothy, J.; 112 Bacon Street, Natick, MA 01670 (US). JUDY, Michael, W.; 95 Chestnut Street, Wakefield, MA 01880 (US).

(74) Agents: CONNORS, Matthew, E. et al.; Samuels, Gauthier & Stevens, LLP, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

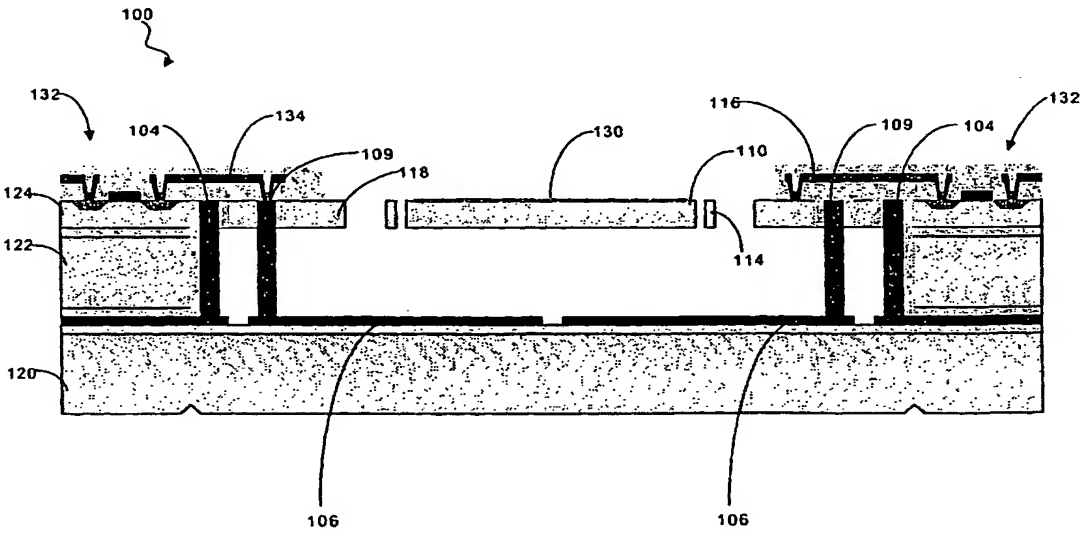
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
4 April 2002

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: BONDED WAFER OPTICAL MEMS PROCESS




(57) Abstract: A microelectromechanical system is fabricated from a substrate having a handle layer, a silicon sacrificial layer and a device layer. A micromechanical structure is etched in the device layer and the underlying silicon sacrificial layer is etched away to release the micromechanical structure for movement. One particular micromechanical structure described is a micromirror.

WO 02/12116 A3

# INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 01/41523

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81B3/00 B81B7/02 G02B26/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81B G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | DE 198 47 455 A (BOSCH GMBH ROBERT)<br>27 April 2000 (2000-04-27)<br>figures 4-11<br>column 8, line 61 -column 11, line 31 | 1,3,19,<br>21,27,32 |
| A | | 2,4-18,<br>20,<br>22-26,<br>28-31,<br>33-42 |
| | --- | |
| X | EP 0 834 759 A (MCNC)<br>8 April 1998 (1998-04-08)<br>figures 1-5<br>column 2, line 27 -column 5, line 47<br>column 6, line 43 -column 13, line 25 | 23-26 |
| A | | 1-22,<br>27-42 |
| | --- | |
| | -/-- | |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 4 February 2002 | 11/02/2002 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Polesello, P |

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
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| A | | 3-18,20,<br>22,<br>28-32,<br>35-42 |
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| A | | 3,5,<br>7-18,<br>20-42 |
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| A | | 3-18,20,<br>22-42 |
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| | ----- | |

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Information on patent family members

Internat .l Application No
PCT/US 01/41523

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